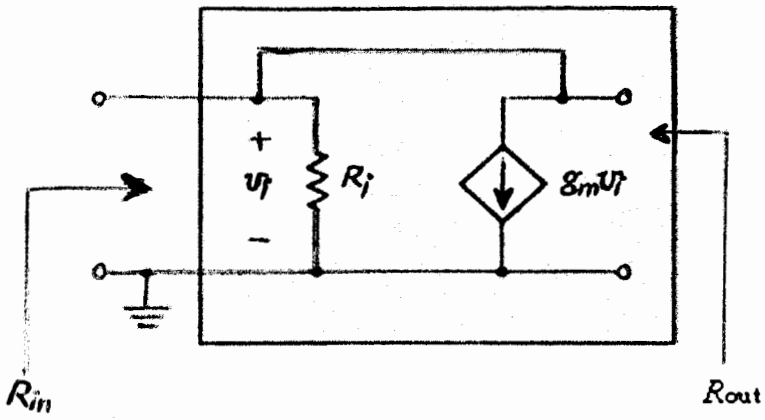
系所組別：工程科學系甲、戊、己組

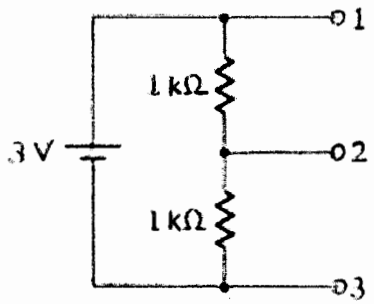
考試科目：電子電路

※ 考生請注意：本試題可使用計算機

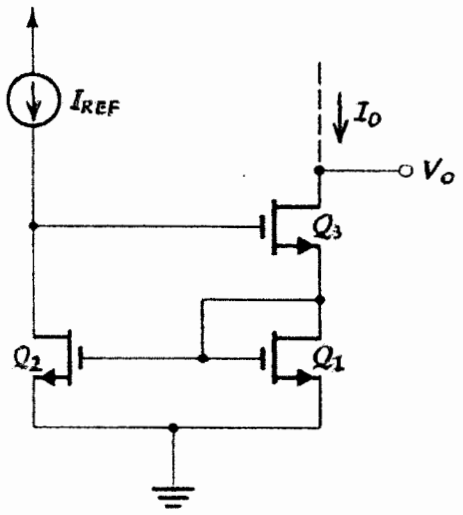
1. (a) Find the input and output resistances. Notice that when determining R_{out}, v_i should be removed (or shorted). (10 分)



(b) Find the Thevenin and Norton equivalent circuits between terminals 1 and 2. (5 分)



2. (1) Determine the output resistance of the Wilson MOS mirror. Note that output resistances of MOS, r_o, **cannot** be ignored. (10 分) (2) Determine the current transfer ratio. Note that output resistances of MOS, r_o, **can** be ignored. (10 分)



(背面仍有題目，請繼續作答)

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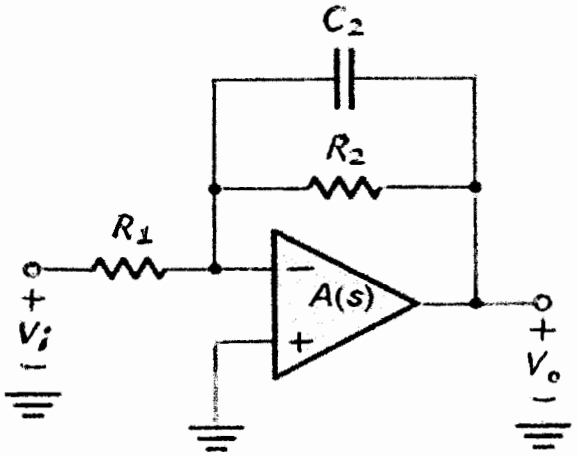
3. A commercial μA741 is employed in the noninverting configuration, $R_1 = 1\ k\Omega$, $R_2 = 9\ k\Omega$, and $C_2 = 100\ \text{nF}$. The op amp has its open-loop gain (or transfer function) as $A(s)$.

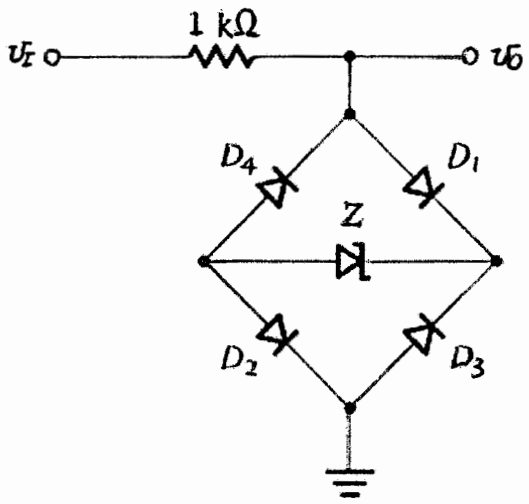


(a) If the op amp is ideal and has an infinite open-loop gain, $A(s) = \infty$, find the closed-loop gain, $G(s)$. (5 分)

(b) If the op amp is ideal except that its open-loop gain is finite, $A(s) = \dfrac{10^4}{1 + \dfrac{s}{2\pi \times 100}}$, find the closed-loop gain, $G(s)$. (5 分)

(c) Plot the magnitude plot of $G(s)$ in (a). (5 分)

4. This is a limiter circuit. All diodes in forward region can be represented by a constant-voltage drop of 0.7V. The specified zener voltage 8.2 V is measured in breakdown region with a current of 10 mA and that $r_z = 100\ \Omega$, represent the zener by a piecewise-linear model. Sketch and clearly label the transfer characteristic for $-20\ \text{V} \le v_I \le 20\ \text{V}$ by considering three cases (a) $I_{ZK} = 0\ \text{mA}$ (5 分) (b) $I_{ZK} = 20\ \text{mA}$ (5 分) (c) $I_{ZK} = 400\ \text{mA}$. (5 分)



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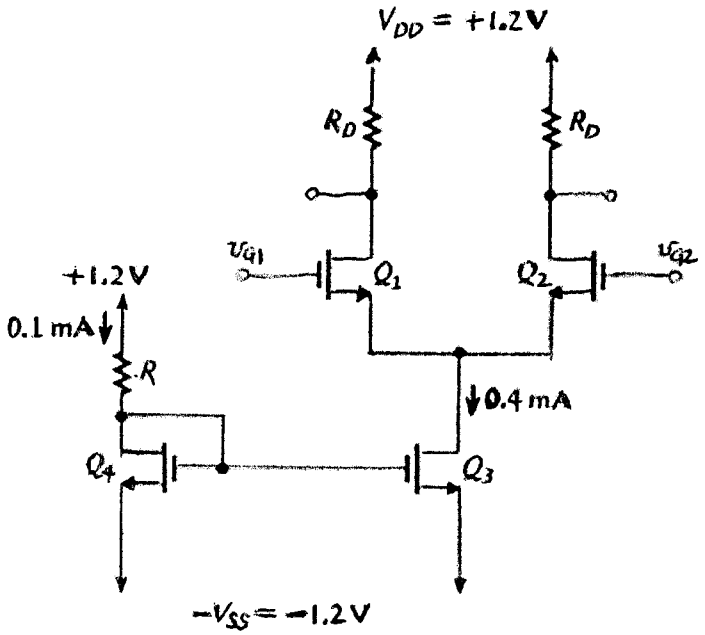
5. Design the circuit to obtain a dc voltage of +0.2V at each of the drains of Q_1 and Q_2 when $v_{G1} = v_{G2} = 0$V. Operate all transistors at V_{ov}=0.2 V and assume that for the process technology in which the circuit is fabricated, V_{tn}= 0.5V and $\mu_n C_{ox}$= 250 μA/V^2. Neglect channel-length modulation. (1) Determine the values of R, R_D, and the W/L ratios of Q_1, Q_2, Q_3, and Q_4. (12 分) (2) What is the input common-mode voltage range for your design? (8 分)



6. For the feedback amp, if the op amp has an open-loop gain μ and a very large input resistance, find $A_f \equiv I_o/V_s$, A, and $\beta \equiv V_f/I_o$. (15 分)