國立成功大學 105 學年度碩士班招生考試試題

編號: 127

系 所:工程科學系 考試科目:電子電路

考試日期:0228,節次:1

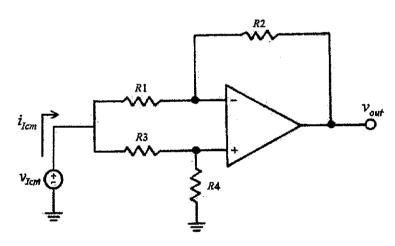
第1頁,共2頁

※ 考生請注意:本試題可使用計算機。 請於答案卷(卡)作答,於本試題紙上作答者,不予計分。**證** 依題號順序作答。

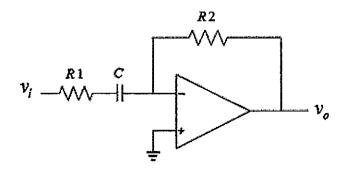
1. A device is characterized by its current i_D (mA) and voltage v_D (V) as $i_D = K(1+v_D)^3$, where K=1 mA/V³. (a) Find its small-signal equivalent model (10 pt.). (b) If the DC voltage $V_D=2$ V, find the DC current I_D and the transconductance g_m . (10 pt.)

2. In the following circuit, (a) if R1=1 k Ω , R2=2 k Ω , R3=4 k Ω , and R4=2 k Ω , find v_{out} expressed by v_{lcm} (5 pt.); (b) if R1=1 k Ω , R2=2 k Ω , R3=4 k Ω , and R4=2 k Ω , find $R_{lcm} = \frac{v_{lcm}}{i_{lcm}}$ (5 pt.); (c) if R1=R3=1 k Ω and

 $R2=R4=2 \text{ k}\Omega$, find v_{out} expressed by v_{Icm} (5 pt.); (d) if $R1=R3=1 \text{ k}\Omega$ and $R2=R4=2 \text{ k}\Omega$, find $R_{Icm} \equiv \frac{v_{Icm}}{i_{Icm}}$ (5 pt.).



3. The following circuit performs the high-pass, single-time-constant function. Such a circuit is known as a first-order high-pass active filter. (a) Design the circuit to obtain a high-frequency input resistance of 100 kΩ, a high-frequency gain of 40 dB, and a 3-dB frequency of 100 kHz. (15 pt.) (b) At what frequency does the magnitude of the transfer function reduce to unity? (5 pt.)



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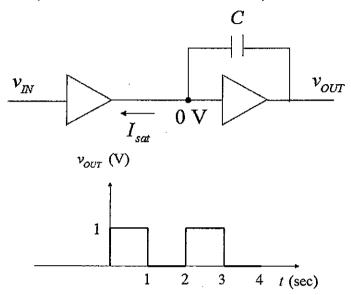
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4. The figure shows a two-stage amp, the 1st stage saturates owing to the large input voltage, where $I_{sat} = 0.1 \text{ mA}$ and $C = 100 \ \mu \text{ F}$. (a) Find the slew rate. (5 pt.) (b) If the ideal output is a square wave shown below, plot the real output waveform which is distorted by the slew rate. (10 pt.)



5. For the circuit shown below, assume $V_t = 1.5 \, \mathrm{V}$, $V_A = \infty \, \mathrm{V}$, and $k_n' \left(\frac{W}{L} \right) = 0.25 \, \mathrm{mA/V^2}$. Find (a) DC operating point. (5 pt.) (b) Its small-signal voltage gain. (5 pt.) (c) The amplitude of the largest allowable input signal and the minimum allowable v_{DS} , i.e., $v_{DS,\mathrm{min}}$. (5 pt.) (d) Please change the resistance of R_D such that the DC drain voltage $V_D = \frac{V_{DD} + v_{DS,\mathrm{min}}}{2}$, where $v_{DS,\mathrm{min}}$ denotes the minimum allowable v_{DS} obtained in (c). (5 pt.) (e) Also, find the amplitude of the largest allowable input signal and the new minimum allowable v_{DS} , i.e., $v_{DS,\mathrm{min}}'$ in this case again. (5 pt.)

