編號： 122

國立成功大學 108 學年度碩士班招生考試試題

系　　所：工程科學系

考試科目：電子電路

考試日期：0224，節次：1

※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Mark each of the following statements True (T) or False (F). (Need NOT give reasons.) (20 pt.)

(a) The typical diode can never work in the breakdown region except the Zener diode.

(b) When typical diodes work in the breakdown region, they will definitely break down.

(c) Diodes can be applied for the rectifier and limiter circuits.

(d) The small-signal model of a typical diode in the forward region is a resistance.

(e) The small-signal model of the Zener diode in the breakdown region is a DC voltage plus a resistance.

(f) The power used for the amplification of a signal mainly comes from the AC power.

(g) The input terminals of an OP AMP are virtual shorted because their input currents are zero.

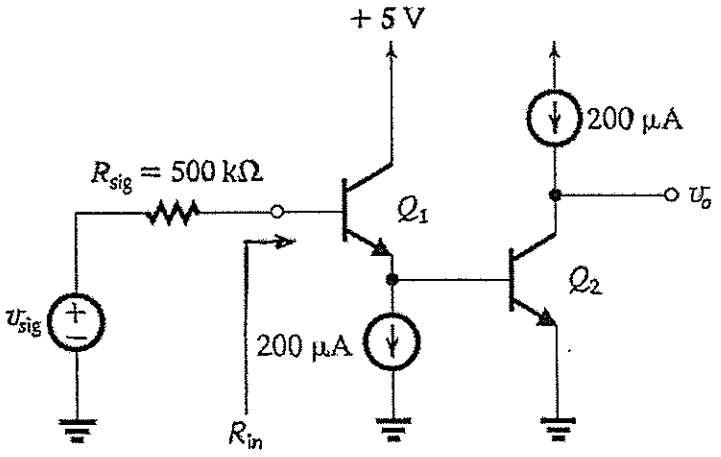
(h) If we need a closed-loop gain which is finite and predictable, the very high gain of an OP AMP makes it impossible to use by itself.

(i) When designing an amplifier, there typically exists a tradeoff between gain and bandwidth.

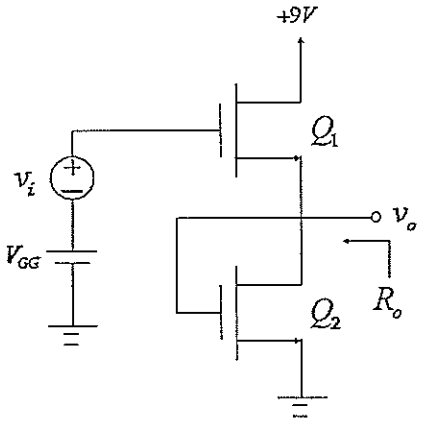
(j) The supply electricity of the wall outlet in Taiwan is 110 V, which represents the peak amplitude of the electricity.

2. A transmission line has a voltage drop of 10% and resistance of 10 Ω. (a) Find the root-mean-square (rms) amplitude of the current flowing through the transmission line for AC supply of 200 V peak amplitude. (b) Find the line loss, i.e., the power consumed in the transmission line. (10 pt.)

3. The transistors in the circuit have $\beta = 100$ and $|V_A| = 50$ V. Find R_{in} and the overall voltage gain $A_v \equiv v_o / v_{sig}$. (20 pt.)



4. In the circuit, Q_1 and Q_2 have following parameters: $k_n'\left(\frac{W}{L}\right)_1 = 2\ \text{mA/V}^2$, $k_n'\left(\frac{W}{L}\right)_2 = 0.2\ \text{mA/V}^2$, $V_{t1} = V_{t2} = 1\ \text{V}$, and $\lambda = 0$. Find (a) V_{GG} that makes V_{DS2} of Q_2 be 4 V. (b) $A_v \equiv \frac{v_o}{v_i}$. (c) R_o. (d) The maximum allowable input amplitude of v_i. (Hint: Besides saturation, you must also guarantee voltages at all nodes are not larger than $V_{DD} = 9\ \text{V}$.) (30 pt.)



5. A MOS differential pair with the drain resistors R_D implemented using diode-connected PMOS transistors, Q_3 and Q_4, as shown below. Let Q_1 and Q_2 be matched, and Q_3 and Q_4 be matched as well. Assume $g_{m1} = g_{m2} = g_{m3} = g_{m4} = 1\ \text{mA/V}$ and $r_{o1} = r_{o2} = r_{o3} = r_{o4} = 10\ \text{k}\Omega$, find the differential gain $A_d \equiv v_o / v_{id}$. (20 pt.)