1. (a) For the circuit in Fig. 1, assume high β and BJTs having $V_{BE} = 0.7\,V$ at 1 mA. Find the value of R that will result in $I_o = 10\,\mu A$. (10分)

(b) For the design in (a), find R_o assuming $\beta = 100$ and $V_A = 100\,V$. (10分)

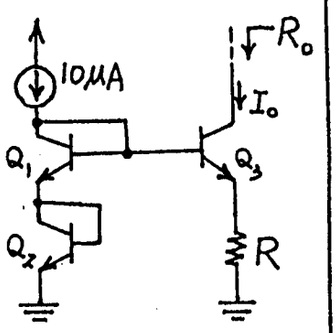

Fig. 1

2. For the circuit in Fig. 2, $|V_t| = 1\,V$, $K = 0.5\,mA/V^2$, $h_{fe} = 100$, and the Early voltage magnitude for all devices (including those that implement the current sources) is 100 V. The signal source V_s has a zero dc component.

(a) Find the dc voltage at the output. (3分)

(b) Find the dc voltage at the base of Q_3. (2分)

(c) Find the voltage gain, V_o/V_s. (15分)

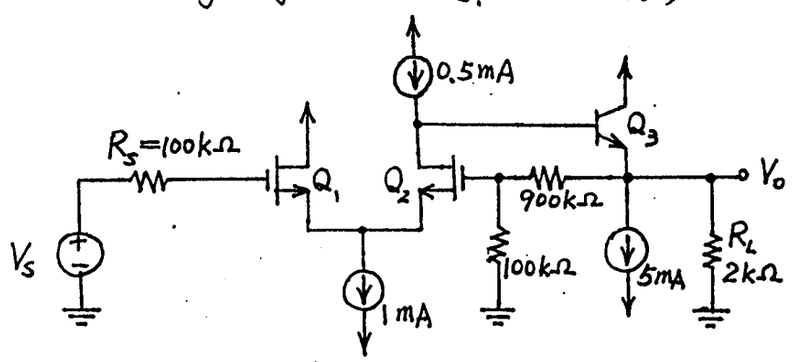

Fig. 2

3. For each circuit in Fig. 3, derive an equation governing circuit operation, and find the frequency of oscillation and gain condition that ensures that oscillations start. (20分)

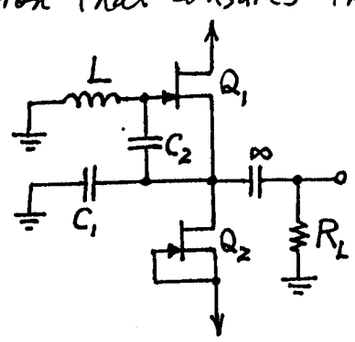

Fig. 3(a)

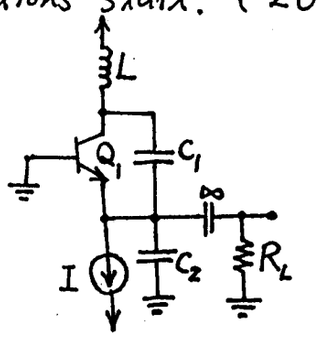

Fig. 3(b)

4. For each circuit in Fig. 4, determine $\frac{V_o(s)}{V_i(s)}$. (20分)

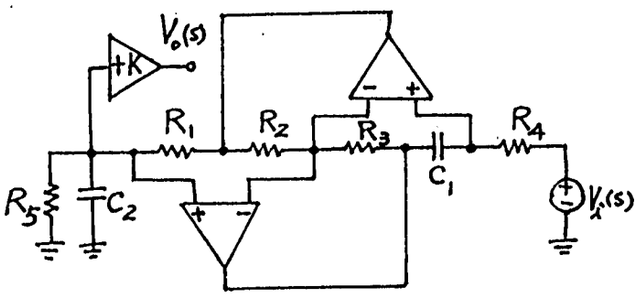

Fig. 4(a)

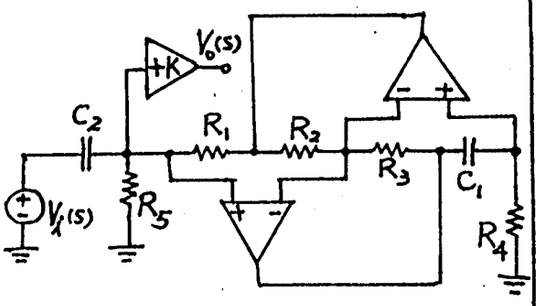

Fig. 4(b)

5. The circuit shown in Fig. 5 uses an op amp having a ±5-mV offset.

(a) What is its output offset voltage? (6分)

(b) What does the output offset become with the input ac coupled through a capacitor C? (6分)

(c) If, instead, the 1-kΩ resistor is capacitively coupled to ground, what does the output offset become? (8分)

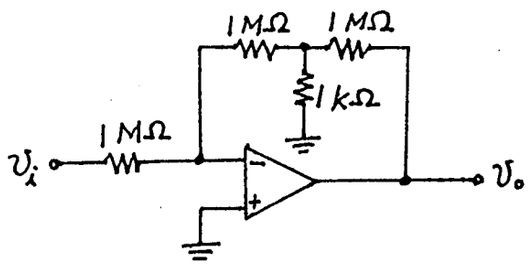

Fig. 5