图学年度 國立成功大學工程科学系 电子电路 試題 共一頁

請按題號順序作答 (每題分數 20 分)

- 1. In the circuit of Fig. 1, the NMOS transistor has $|V_i| = 0.9 \text{ V}$ and $|V_a| = 50 \text{ V}$, and operates with $|V_o| = 2 \text{ V}$.
 - (a) What is the voltage gain v_{α}/v_{z} ?
 - (b) What do V_n and the gain become for I increased to 1 mA?
- 2. For the differential amplifier shown in Fig. 2, find
 - (a) the differential gain,
 - (b) the differential input resistance,
 - (c) the common-mode gain, and
 - (d) the common-mode input resistance.
- 3. A class AB output stage using a two-diode bias network as shown in Fig. 3 utilizes diodes having the same junction area as the output transistors. For V_{Cl} = 10 V, I_{bias} = 0.5 mA , R_L = 100 Ω , β_N = 50 , and |V_{Clisat}| = 0 V, what is the quiescent current? What are the largest possible positive and negative output signal levels? To achieve a positive peak output level equal to the negative peak level, what value of β_N is needed if I_{bias} is not changed? What value of I_{bias} is needed if β_N is held at 50?
- 4. For the circuits in Figs. 4(a) to 4(c), sketch and label the transfer characteristic v_O v_I. Denoting the zener voltages of Z₁ and Z₂ by V_{Z1} = 6 V and V_{Z2} = 4 V and assuming that in the forward direction the voltage drop is approximately 0.7 V. The diodes are assumed to have a constant 0.7 V drop when conducting. The op amp saturates at ±12 V.
- Design a Chebyshev filter that meets the following low-pass specifications: f_p = 3.4 kHz, f_s = 4 kHz,
 A_{max} = 1 dB, and A_{max} = 35 dB. Find the required order N, the poles, and the transfer function T(s).

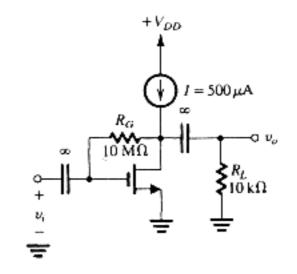


Fig. 1

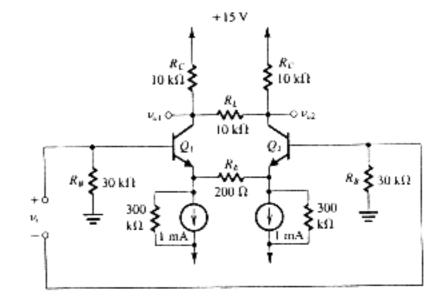


Fig. 2

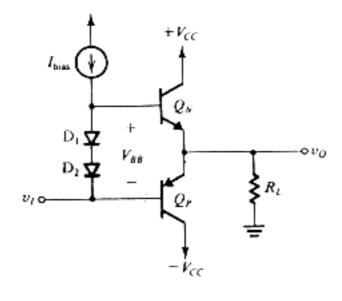
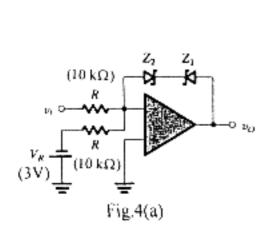
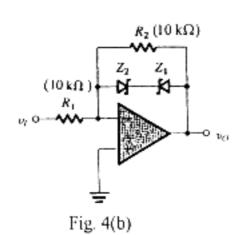


Fig. 3





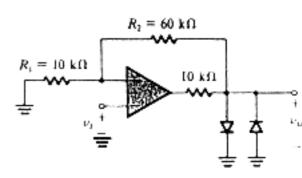


Fig. 4(c)