1. Find and sketch the voltage transfer characteristic of the circuit shown in Fig. 1, assuming that the diodes have a constant 0.7 V drop when conduct. (15 分)

2. The CMOS circuit is shown in Fig. 2 for which Q_1 has parameters g_{m1} and r_{o1} and Q_2 has g_{m2} and r_{o2}. Find

   $A_V = V_o / V_s$. (15 分)

3. For the CMOS monostable circuit shown in Fig. 3, sketch v_{o1}, v_{o2}, v_R and determine the pulse duration. (15 分)

4. A circuit is shown in Fig. 4, determine the value of v_O. (15 分)

5. For the circuit in Fig. 5 in which the transistors have $V_{BE} = 0.7$ V and $\beta = 100$, find v_o / v_i and R_{in}. (20 分)

6. An amplifier having a low-frequency gain of 10^3 and poles at 10^4 and 10^5 Hz is operated in a closed negative-feedback loop with a frequency-independent β.

   (a) For what value of β do the closed-loop poles become coincident? At what frequency? (7 分)
   (b) What is the low-frequency gain corresponding to the situation in (a)? (3 分)
   (c) What is the value of pole Q factor corresponding to the situation in (a)? (3 分)
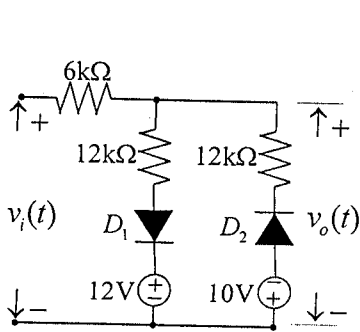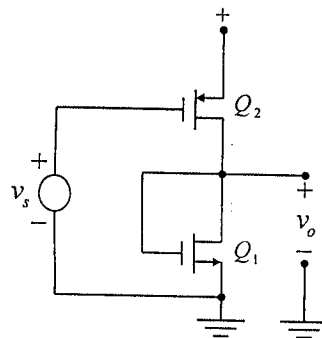   (d) If β is increased by a factor of 10, what are the new pole locations? What is the corresponding pole Q factor? (7 分)
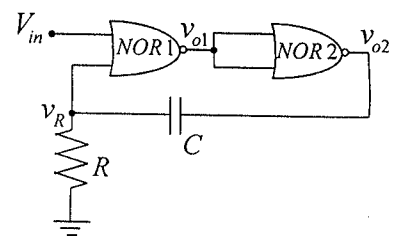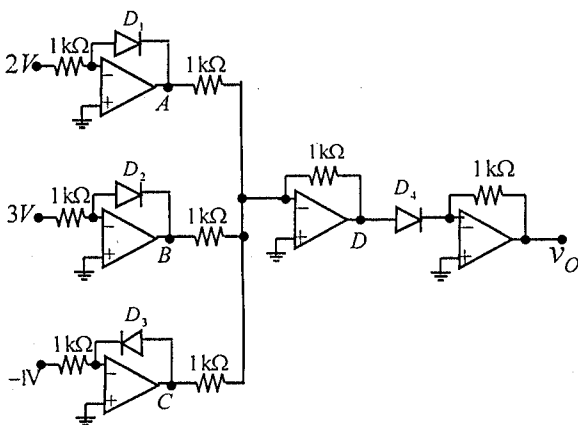

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5