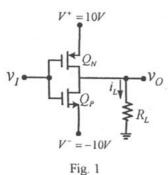
9D 學年度 國立成功大學 工程科學系 電子電路 試題 共一頁 碩士班招生考試 (田·成) 所 電子電路 試題 第一頁

請按題目順序作答

- 1. Consider the class-B output stage shown in Fig. 1. The transistor parameters are $|V_{th}| = 0$ and $k'_n = k'_p = 0.4 \text{ mA/V}^2$. Let $R_t = 5 \text{ k}\Omega$.
- (a) Find the maximum output voltage such that Q_N remains biased in the saturation region. What are the corresponding values of i_L and ν_I for this condition? (8分)
- (b) Determine the conversion efficiency for a symmetrical sine-wave output signal with the peak value found in part (a). (8分)



2. Consider the current-to-voltage converter circuit shown in Fig. 2. The input resistance R_{ij} is assumed to be small, the output resistance is $R_o = 0$, and the op-amp gain A is large. The closed-loop transfer function can be written in the form

$$A_f = \frac{v_o}{i_s} = \frac{A}{1 + A\beta}$$

- (a) What is the expression for β . (8分)
- (b) If $A = 5 \times 10^6 \ \Omega$ and $A_f = 5 \times 10^4 \ \Omega$, what is the required R. (8 %)

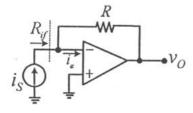


Fig. 2

3. Find the frequency of oscillation and the R_2/R_1 required for oscillation for the circuit shown in Fig. 3. (16 分)

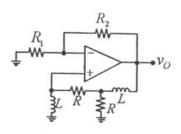
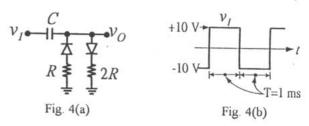


Fig. 3

4. For the circuit in Fig. 4(a), utilizing ideal diodes, determine and sketch the output $v_o(t)$ for the input $v_1(t)$ shown in Fig. 4(b). Assume CR = T. (16 $\frac{1}{2}$)



- 5. An amplifier is formed by cascading n identical amplifier stages, each having a high-pass single-time-constant frequency response with a 3-dB frequency f_1 and a low-pass single-time-constant frequency response with a 3-dB frequency f_2 . Find the lower 3-dB frequency and upper 3-dB frequency of the overall amplifier in terms of f_1 , f_2 and g_2 . (18 f_2)
- 6. (a) Sketch a CMOS realization for the function $Y = \overline{A + B(C + DE)}$. (b) Sketch a CMOS logic circuit that realizes the function $Y = ABC + \overline{A} \, \overline{B} \, \overline{C}$. (18 $\frac{1}{12}$)