編號:

144

國立成功大學九十八學年度碩士班招生考試試題

共分頁,第1頁

系所組別: 工程科學系甲、戊、己組

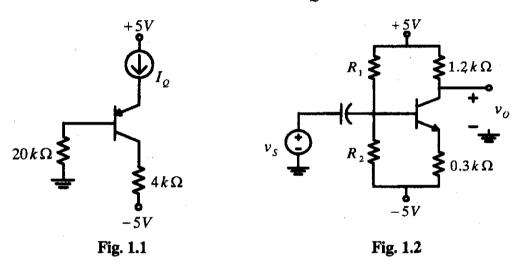
考試科目: 電子電路

考試日期:0307,節次:1

※ 考生請注意:本試題 ☑可 □不可 使用計算機

1. (15%) (a) (7%) The circuit shown in Fig. 1.1 is biased with a constant-current source I_Q . The transistor has $\beta=120$ and the E-B turn-on voltage is $V_{EB}(on)=0.65V$. Determine I_Q such that $V_{ECQ}=3V$.

(b) (8%) Consider the circuit with $\beta = 120$ and $V_{BE}(on) = 0.7V$ as shown in Fig. 1.2. Design R_1 and R_2 such that $V_{CEQ} = 5V$.



2. (20%) A feedback amplifier is shown in Fig. 2. Assume that all transistors are matched and that $V_T = 25mV$, $\beta = 100$ (of the BJT), $I_{C_1} = I_{C_2} = 1.0mA$ and $r_o = \infty$. Please determine (a) (5%) g_m , r_e , r_π ; (b) (5%) the voltage gain v_2/v_1 ; (c) (5%) the input resistance R_i ; (d) (5%) the output resistance R_o .

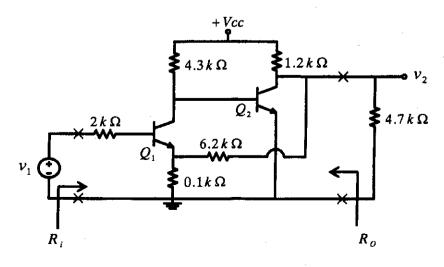


Fig. 2

(背面仍有題目,請繼續作答)

編號:

144

國立成功大學九十八學年度碩士班招生考試試題

共う頁 第2頁

系所組別: 工程科學系甲、戊、己組

考試科目: 電子電路

考試日期:0307, 節次:1

※ 考生請注意:本試題 ☑可 □不可 使用計算機

3. (15%) Consider the circuit shown in Fig. 3. The two port circuit A has the hybrid parameters: $h_{11}=1\Omega$, $h_{12}=\frac{1}{3}$, $h_{21}=-3$ and $h_{22}=\frac{1}{3}\Omega^{-1}$. Please determine (a) (5%) the voltage gain V_1/V_2 ; (b) (5%) the voltage V_2 ; (c) (5%) the input resistance R_i .

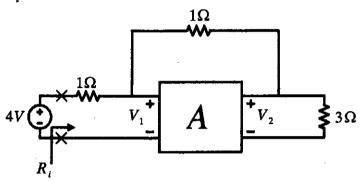


Fig. 3

4. (15%) Assume that the OP amp and diodes are ideal in the circuit of Fig. 4. (a) (8%) Please plot the transfer chacteristic (v_o with respect to v_i) of the circuit. (b) (7%) If $v_i(t) = 5\sin(2\pi t)$, please plot the output voltage $V_o(t)$ in the time domain.

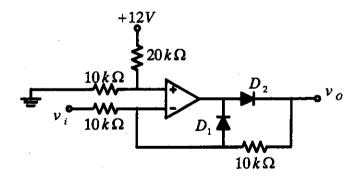


Fig. 4

5. (15%) (a) (10%) Assume that the op amp is ideal and all initial conditions are zero in the circuit of Fig. 5. (i) (5%) Please determine the transfer function $\frac{V_o(S)}{V_i(s)}$ of

the circuit. (ii) (5%) Please derive the input-output differential equation in the time domain.

(b) (5%) Please design an analog circuit to solve the following differential equation (all initial conditions are zero)

編號:

國立成功大學九十八學年度碩士班招生考試試題

共子頁,第子頁

系所組別: 工程科學系甲、戊、己組

考試科目: 電子電路

144

考試日期:0307・節次:1

※ 考生請注意:本試題 ☑可 □不可 使用計算機

$$\frac{d^{2}v_{o}(t)}{dt} + \frac{dv_{o}(t)}{dt} + v_{o}(t) = 1.$$

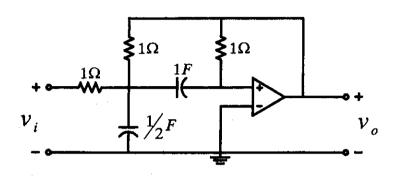


Fig. 5

- 6. (20%) Consider the differential amplifier in the **Fig. 6**, the component's characteristic as following, Q_1 and Q_2 are matched JFETs with $I_{DSS}=2.5~mA$, $V_P=-2~V$ and Q_3 is the BJT with $\beta=\infty$. The input voltages of the JFETs, represented by v_{S1} and v_{S2} , are only small signal without DC component.
 - (a) (10%) Find the DC quiescent point $(I_{15.3k\Omega}, I_{C3}, V_{C3})$ and V_{D2} .
 - (b) (10%) Determine the small signal voltage gain if the output is taken differentially. ($r_O = \infty$ for all the JFETs and BJT).

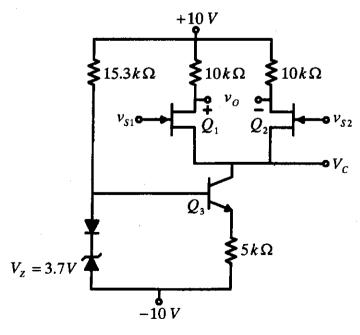


Fig. 6