

# 國立成功大學

## 113學年度碩士班招生考試試題

編 號： 127

系 所： 系統及船舶機電工程學系

科 目： 電子學

日 期： 0201

節 次： 第 2 節

備 註： 可使用計算機

※ 考生請注意：本試題可使用計算機。請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

- The circuit in Fig. 1 utilizes an ideal op amp. (20%)

  - Find  $I_1, I_2, I_3, I_L$ , and  $V_X$ .
  - If  $V_0$  is not to be lower than  $-13\text{ V}$ , find the maximum allowed value for  $R_L$ .
  - If  $R_L$  is varied in the range  $100\Omega$  to  $1\text{ k}\Omega$ , what is the corresponding change in  $I_L$ , and in  $V_0$ ?
- In the Fig. 2, Design a diode voltage regulator to supply  $1.5\text{ V}$  to a  $1.5\text{ k}\Omega$  load. Use two diodes specified to have a  $0.7\text{ V}$  drop at a current of  $1\text{ mA}$ . The diodes are to be connected to a  $+5\text{ V}$  supply through a resistor  $R$ . **Specify the value for  $R$ .** (a)What is the diode current with the load connected? (b)What is the increase resulting in the output voltage when the load is disconnected? (c)What change results if the load resistance is reduced to  $1\text{ k}\Omega$ ? (Hint: Use the small-signal diode model to calculate all changes in output voltage.) (20%)
- The MOSFET in Fig. 3 has  $V_t=0.4\text{ V}$ ,  $k_n'=500\mu\text{A/V}^2$  and  $\lambda=0$ . Find the required values of  $W/L$  and of  $R$  so that when  $v_i = V_{DD} = +1.3\text{ V}$ ,  $r_{DS}=50\Omega$  and  $v_0 = 50\text{ mV}$ . (20%)

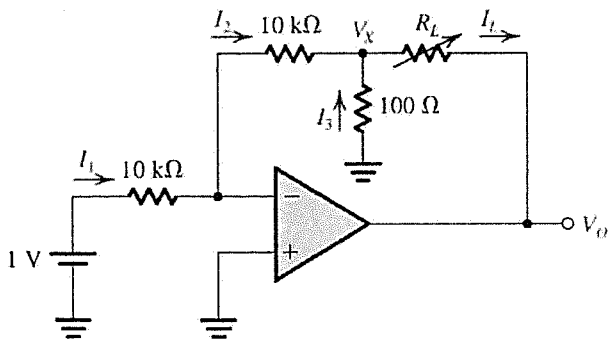


Fig. 1

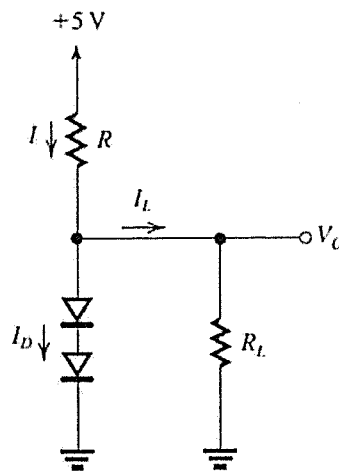


Fig. 2

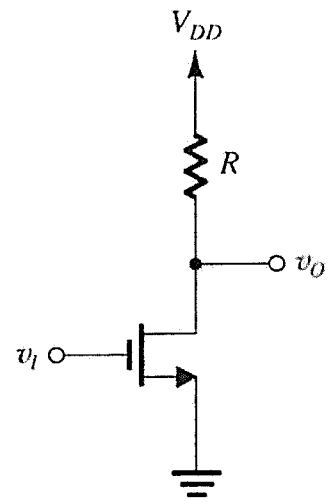


Fig. 3

4. The amplifier of Fig. 4 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage,  $R_{in2}$ , constitutes the load resistance of the first stage. (20%)
- (a) For  $V_{CC}=15V$ ,  $R_1=100k\Omega$ ,  $R_2=47k\Omega$ ,  $R_E=3.9k\Omega$ ,  $R_C=6.8k\Omega$ , and  $\beta=100$ , determine the dc collector current and dc collector voltage of each transistor.
- (b) Find  $R_{in1}$  and  $v_{b1}/v_{sig}$  for  $R_{sig} = 5 k\Omega$ .
- (c) Find  $R_{in2}$  and  $v_{b2}/v_{b1}$ .
- (d) Find the overall voltage gain  $v_o/v_{sig}$  for  $R_L=2 k\Omega$ .

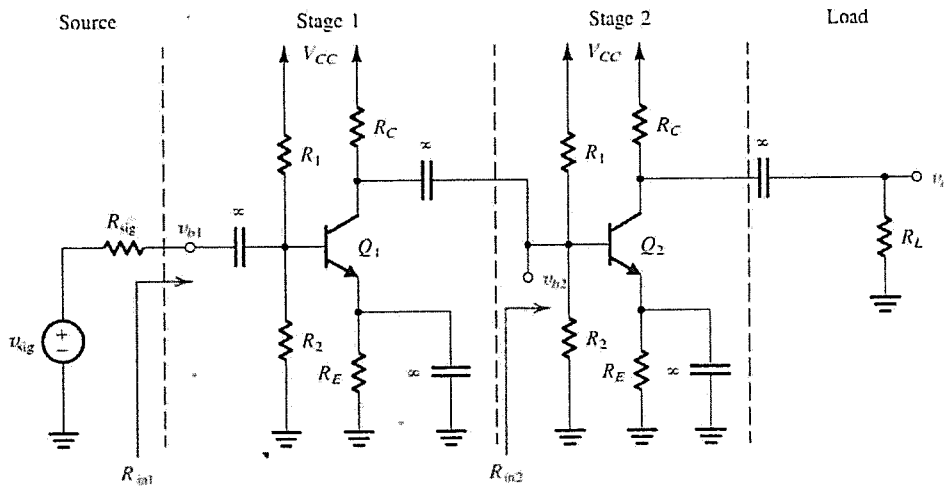


Fig. 4

5. The amplifier in Fig. 5 is biased to operate at  $g_m=2mA/V$ . Neglect  $r_o$ . (20%)
- (a) Determine the value of  $R_D$  that results in a midband gain of  $-20 V/V$ .
- (b) Determine the value of  $C_S$  that results in a pole frequency of 100 Hz.
- (c) What is the frequency of the transmission zero introduced by  $C_S$  ?
- (d) Give an approximate value for the 3 dB frequency  $f_L$

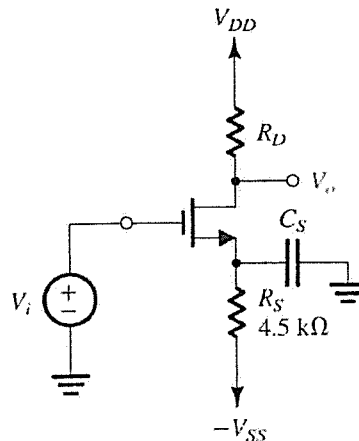


Fig. 5