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(一). 50%

Select the most appropriate answers for the following multiple choice problems. Each problem may have more than one answer. Five point each, no partial point, no penalty.

1. Which of the following is (are) true?
   (a) Caches can be used to store instructions as well as data. An instruction cache is accessed at a latter pipeline stage called MEM.
   (b) For a cache memory of some fixed size, the larger the cache block size is the smaller the tag memory the cache uses.
   (c) For a direct-mapped cache, since a cache block is addressed by the different index value, therefore no address tag is the same in the tag memory.
   (d) For a two-way set associative cache, two cache blocks are indexed at the same time.

2. Which of the following is (are) true for the forwarding unit used in a typical five-stage pipelined processor?
   (a) The forwarding unit is used to bypass the write-back result due to RAW hazards.
   (b) The forwarding unit is used to forward data to the instruction cache.
   (c) The forwarding unit compares the source register number of the instructions in the MEM and WB stages with the destination register numbers of the dependent instruction.
   (d) The forwarding unit compares the destination register number of the instructions in the MEM and WB stages with the source register numbers of the dependent instruction

3. Which of the following is (are) true?
   (a) A control hazard occurs due to the need to determine the proper instruction to fetch in the MEM stage of a pipeline processor.
   (b) A control hazard occurs due to the need to determine the proper instruction to fetch in the IF stage of a pipeline processor.
   (c) The need to flush instructions in the pipeline due to a control hazard comes from the misprediction of the PC.
   (d) A branch history buffer is typically indexed by the load instruction address.

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4. Which of the following is (are) true for a TLB?
   (a) A TLB is a cache for instruction and data.
   (b) A TLB is a register for virtual page number.
   (c) A TLB is a cache for page table.
   (d) It is possible that an instruction access results in an instruction TLB miss and a page table hit.
5. Which of the following is (are) true?
   (a) Virtual memory technique treats the main memory as a fully-set associative write-back cache.
   (b) Using virtual memory technique can improve process protection.
   (c) A process has its own virtual address space.
   (d) A running process is swapped to disk entirely when new pages are moved into the main memory.

6. Which of the following is (are) true?
   (a) For CPU time, compiler affects the CPI (clocks per instruction) as well as the instruction count used.
   (b) Dynamic power = Capacitive load × Voltage × Frequency switched
   (c) Good yield means a high percentage of good dies out of the total number of dies on the wafer.
   (d) Processor die yield is closely related to the processor architecture.

7. Which of the following is (are) true?
   (a) Processor ISA means the instruction set architecture of the processor.
   (b) ISA is an abstraction which enables different implementations of the same ISA to run identical software.
   (c) For CPU time, ISA affects the CPI.
   (d) For CPU time, ISA affects the instruction count to use also.

8. Which of the following is (are) true?
   (a) A page fault is signaled by hardware.
   (b) A TLB exception can also result in a page fault.
   (c) A cache miss is typically handled by software.
   (d) A page fault is typically handled by hardware.

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9. Which of the following is (are) true?
   (a) Write-allocate policy means when a cache write miss occurs, the written data are updated in the next level of memory.
   (b) There is no cache coherency problem for the write-through cache since the data are written into the next level of memory, and thus the data are consistent between the two caches.
   (c) A cache can be a shared cache or a private cache.
   (d) A cache can use either virtual address or physical address for its tag.

10. Which of the following is (are) true?
   (a) A C compiler is a software tool which compiles a C program into the assembly language program for the target processor.
   (b) Pseudo instructions are instructions which are not implemented in hardware, so they cannot be used in assembly programming.
   (c) A label used in assembly program is also a pseudo instruction.
   (d) Pseudo instructions are directives for assembler in an assembly language program.

(二). 20%

Assume there are three small caches, each consisting of four one-word blocks. One cache is fully associative, a second is two-way set-associative, and the third is direct-mapped. Find the number of misses for each cache organization given the following sequence of block addresses: 0,8,0,6, and 8.

(三). 10%

(a) Virtual machines were developed in mid-1960s, but largely ignored in the domain of single-user computers in the 1980s and 1990s. Please describe why do they have recently gained popularity?

(b) Please describe the benefits that the virtual machines can provide.

(c) Please explain the requirements of a virtual machine monitor.

(四). 20%

In a memory hierarchy like of Figure 1, which includes a TLB and a cache organized as shown, a memory reference can encounter three different types of misses: a TLB miss, a page fault, and a cache miss. Consider all the combinations of these three

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events with one or more occurring (seven possibilities). For each possibility, state whether this event can actually occur and under what circumstances.

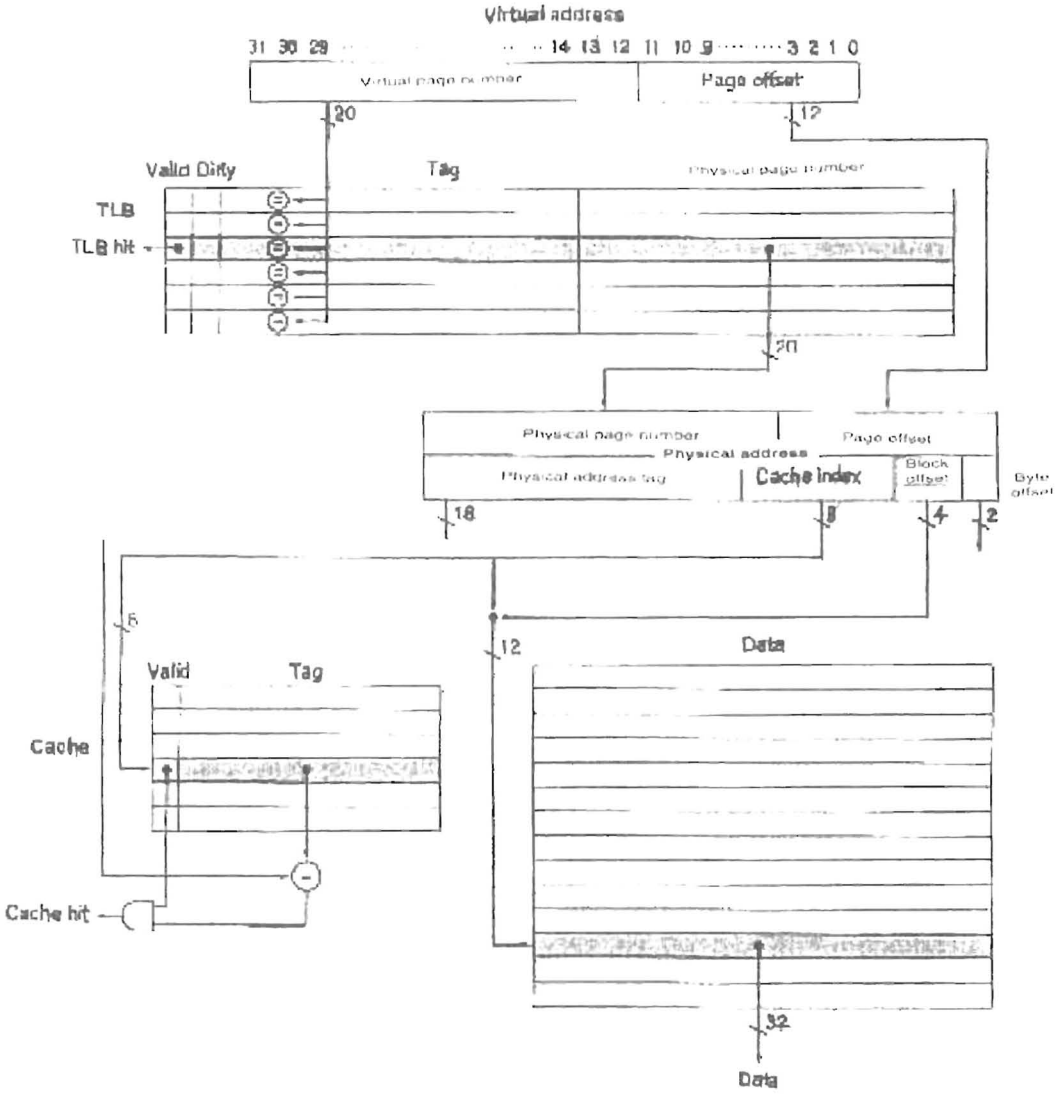

Figure 1. The TLB and cache implement the process of going from a virtual address to a data item in the Intrinsity FastMATH. This figure shows the organization of the TLB and the data cache, assuming a 4 KB page size and a 32-bit address space. This diagram focuses on a read. The cache is direct mapped, the TLB is fully associative.