(1). For a direct-mapped cache design with 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-4	3-0

a. What is the cache block size (in bytes)? **(4%)**

b. How many entries does the cache have? **(4%)**

c. What is the ratio between total bits required for such a cache implementation over the data storage bits? **(4%)**

d. Starting from power on, the following byte-addressed cache references are recorded. How many blocks are replaced? **(4%)**

Address (in Decimal)	Hex
0	0x 0000 0000
4	0x 0000 0004
16	0x 0000 0010
132	0x 0000 0084
232	0x 0000 00E8
160	0x 0000 00A0
1024	0x 0000 0400
30	0x 0000 001E
140	0x 0000 008C
3100	0x 0000 0C1C
180	0x 0000 00B4
2180	0x 0000 0884

e. What is the hit ratio? **(4%)**

(2). Assume the miss rate of an instruction cache is 1% and the miss rate of the data cache is 3%. If a processor has a CPI of 1 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 30%. **(10%)**

(3). (a) What is TLB, please spell out and explain it? **(5%)**

(b) Why we need TLB in virtual memory? **(5%)**

(4). Describe two replacing schemes used in set-associative cache. **(5%)**

(5). Describe two advantages of virtual memory. **(5%)**

(背面仍有題目,請繼續作答)

(6). Select the most appropriate answers for the following multiple choice questions. Each question may have more than one answer. Five point each, no partial point, no penalty.　　(50%)

1.　Which of the following is (are) true? For a multi-cycle implementation processor,

(a)　an illegal instruction exception is raised by the execution of the instruction when it writes back the result into the destination register.

(b)　an illegal instruction exception is raised by the execution of the instruction when it writes back the result into memory.

(c)　an illegal instruction exception is raised by the execution of the instruction at the execution cycle.

(d)　an illegal instruction exception is raised by the execution of the instruction at the decode cycle.

2.　Which of the following is (are) true regarding the use of a forwarding unit in a typical five-stage pipelined processor?

(a)　The forwarding unit is used to bypass the write-back result due to control hazards.

(b)　The forwarding unit forwards an execution result before it is written back to a destination register.

(c)　The forwarding unit is used to forward data from the instruction cache.

(d)　The forwarding unit snoops the instruction cache access.

3.　Which of the following is (are) true for a cache of 32 KB and 32-byte line size?

(a) If the cacheable address space is 4GB, the tag width uses 17 bits for a direct-mapped structure.

(b) If the cacheable address space is 4GB, the index width uses 16 bits for a direct-mapped structure.

(c) If the cacheable address space is 1GB, the index width uses 10 bits for a direct-mapped structure.

(d) If the cacheable address space is 1GB, the tag width uses 15 bits for a direct-mapped structure.

4.　A pseudo instruction: MOV r1, r2 can be implemented by (using MIPS ISA)

(a)　add r1, r2, r0

(b)　addi r1, r2, 0

(c)　add r2, r1, r0

(d)　sub r1, r0, r2

5.　A MIPS load word instruction is given in the form of " lw r1, offset(rs)."　Which of the following is (are) true?

(a)　For a five stage pipeline, the data address is computed at the memory stage.

(b)　"offset" is a signed number.

(c)　The data TLB is looked up using the data address computed by this load instruction when the virtual memory function is turned on.

(d)　The instruction TLB is looked up using the data address computed by this load instruction when the virtual memory function is turned on.

6.　A MIPS conditional branch instruction is given in the form of " beq r1, r2, L1" Which of the following is (are) true?

(a)　L1 is the absolute memory address of the branch target.

(b)　To form the binary machine code, the value of L1 is computed by the assembler when L1 is an external reference.

(c)　To form the binary machine code, the value of L1 is computed by the linker when L1 is an external reference.

(d)　When the instruction is executed, the binary value of L1 is directly used by the PC of the processor for branch operation.

7.　To achieve " beq r1, r2, L1" in ARM's assembly is done by:　cmp r1, r2, followed by beq L1. Which of the following is (are) true?

(a)　cmp sets the comparison result in register r1.

(b)　cmp sets the comparison result in a condition code register.

(c)　beq L1 compares r1 and r2.

(d)　cmp performs JUMP to L1.

8.　About RAID, which of the following is (are) true?

(a)　RAID 0 can repair one lost disk from its mirror disk.

(b)　RAID 1 can repair all the lost disks from its mirror disks.

(c)　RAID 5 can repair one lost disk from a single parity disk.

(d)　RAID 4 can repair one lost disk from its parity disk.

9.　About virtual memory, which of the following is (are) true?

(a)　A page fault is raised by a TLB miss.

(b)　A page fault is raised by the IF and MEM pipeline stage

(c)　A TLB miss can result in a TLB exception.

(d)　A memory protection violation is raised by a page fault.

10.　About I/O, which of the following is (are) true?

(a)　Programmed I/O is performed by the processor which executes I/O programs.

(b)　Programmed I/O is performed by the DMA controller which executes I/O commands.

(c)　A DMA controller performs I/O operation by the processor.

(d)　A DMA controller performs I/O operations by itself.