系所組別：電機工程學系丁、戊組

考試科目：計算機組織 考試日期：0223，節次：2

※ 考生請注意：本試題不可使用計算機

Choose the correct answers for the following multiple choice problems. Each question may have more than one answer. 10 points each, no partial point, no penalty.

1. Which of the following is (are) true for a 128KB cache with a line size of 64 bytes? Assume that the cacheable memory is 4 GB. Address bits are numbered from A0 to A31
   (a) In a direct-mapped implementation, the index field uses address bit A6 to A16 for cache line selection.
   (b) In a direct-mapped implementation, the tag length is 13 bits.
   (c) In a direct-mapped implementation, the tag length is 15 bits; the field determining the line size is 6 bits in length.
   (d) In a direct-mapped implementation, the total tag size is 30720 bits.

2. Which of the following is (are) true for programmed I/O?
   (a) The transfers of I/O data are performed by a DMA device in the I/O unit.
   (b) The programmed I/O operations are initiated by an interrupt and some special commands.
   (c) The processor executes some load/store instructions and others to transfer the I/O data.
   (d) I/O devices move the data between themselves.

3. Which of the following is (are) true for hazards in a pipelined processor?
   (a) RAW hazard comes from an instruction cache miss.
   (b) Considering two instructions **i** and **j**, with **i** occurring before **j**, **j** tries to read a source before **i** writes it, so **j** incorrectly gets the old value. This is a RAW hazard.
   (c) Considering two instructions **i** and **j**, with **i** occurring before **j**, **j** tries to read a source before **i** writes it, so **j** incorrectly gets the old value. This is a WAR hazard.
   (d) Considering two instructions **i** and **j**, with **i** occurring before **j**, **j** tries to write a destination before it is read by **i** , so **i** incorrectly gets the new value. This is a RAW hazard.

4. Which of the following is (are) true for virtual memory system?
   (a) Virtual memory function can be enabled through software control.
   (b) Virtual memory technique treats part of the main memory as a fully-set associative write-back cache for program execution.
   (c) A translation lookaside buffer can be seen as the cache of a page table.
   (d) A page table is shared among the programs in execution.

5. Which of the following is (are) true as a processor is booted from power-on?
   (a) The program counter value is fetched by the processor from a specified memory location through a load instruction.
   (b) The first instruction is fetched using the program counter value specified by operating system.
   (c) The BIOS provides the address of the first instruction being fetched.
   (d) The first instruction is fetched by the processor using the address specified in the program counter.

(背面仍有題目,請繼續作答)

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6. Which of the following is (are) true about instruction set architecture (ISA)?
   (a) ISA is an abstraction which is the interface between the hardware and the low-level software (assembly instructions).
   (b) ISA enables the different implementations of a processor using the same ISA to run identical software.
   (c) ISA specifies how a processor pipeline should be implemented.
   (d) MIPS and ARM are both RISC-type ISA and use the same instructions set architecture.
7. Which of the following is (are) true about page fault and TLB exception?
   (a) A page fault is signaled by operating system so that the OS can fetch the missing page.
   (b) A TLB exception is handled by the DMA controller in a hard drive.
   (c) Both a page fault and a TLB miss are exceptions and signaled by the processor hardware.
   (d) When a requested page is not found in the main memory, this causes a page fault.
8. Which of the following is (are) true about cache operations?
   (a) When a cache write miss occurs, the written data are directly updated in the next level of memory. This is the write-around policy.
   (b) When a cache write hit occurs, the written data are also updated in the next level of memory. This is the write-through policy.
   (c) There is no cache coherency problem for using the write-through cache since the data are written into the next level of memory.
   (d) Cache is pronounced as [kætʃ].

9. Which of the following is (are) true about the label specified in a branch instruction, for instance, beq r1, r2, **label**?
   (a) The label is a pseudo-instruction and the compiler compiles it into a memory location.
   (b) The label is transformed into an offset specifying the difference between the branch instruction (or the instruction after the branch) and the branch target.
   (c) The label is transformed into an absolute address in memory for the branch target.
   (d) If the label is an external reference, the linker can figure out its value and finalize the binary format for the branch instruction.
10. Which of the following is (are) true?
   (a) Pipelining improves the instruction throughput, i.e., IPC, rather than individual instruction execution time.
   (b) Pipelining improves the instruction throughput, i.e., IPC, other than individual instruction execution time.
   (c) Pipelining improves the instruction throughput, i.e., CPI, rather than individual instruction execution time.
   (d) Pipelining improves the instruction throughput, i.e., CPI, other than individual instruction execution time.