系所組別：電機工程學系丁、戊組

考試科目：計算機組織 考試日期：0222，節次：2

※ 考生請注意：本試題不可使用計算機。 請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

Select the most appropriate answers for the following multiple choice questions (1 to7). Each question may have more than one answer. 10 point each, no partial point, no penalty.

1. Single-Instruction Multiple-Thread (SIMT) microarchitectures implemented in Graphics Processing Units (GPUs) run fine-grained threads in lockstep by grouping them into units, referred to as warps, to amortize the cost of instruction fetch, decode and control logic over multiple execution units. As individual threads take divergent execution paths, their processing takes place sequentially, defeating part of the efficiency advantage of SIMD execution.

Which of the following statements is (are) true ?

a. An SIMT thread runs on the microarchitecture in GPU.
b. A group of SIMT threads which are executed in lockstep are referred to as a warp.
c. "As individual threads take divergent execution paths," this refers to the execution of a conditional instruction.
d. "defeating part of the efficiency advantage of SIMD execution," this means SIMT has better performance than SIMD.

2. For CPUs, the problem of exception support was solved at a relatively early stage. This support was a key enabler to their success, and instrumental in this success was the definition of precise exception handling, where an exception is handled precisely if, with respect to the excepting instruction, the exception is handled and the process resumed at a point consistent with the sequential architectural model.

Which of the following statements is (are) true ?

a. "the exception is handled and the process resumed at a point consistent with the sequential architectural model," this means handling the exception by executing the instruction behind the excepting instruction.
b. "the exception is handled and the process resumed at a point consistent with the sequential architectural model," this means resuming instruction execution at the point behind the excepting instruction.
c. When multiple exceptions occur at the same time, there is only one PC which is stored as the exception PC.
d. The excepting instruction above is also referred to as the faulting instruction.

3. Which of the following is (are) true for a cache of 128 KB and 64-byte line size?

a. If the cacheable address space is 8GB, the tag width uses 10 bits for a direct-mapped structure.
b. If the cacheable address space is 4GB, the index width uses 10 bits for a 2-way set associative structure.
c. If the cacheable address space is 2GB, the line size width bits uses 6 bits for a direct-mapped structure.
d. If the cacheable address space is 16GB, the tag width uses 19 bits for a 4-way set associative structure.

(背面仍有題目,請繼續作答)

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4. Which of the following is (are) true?
a. The target instruction address of an indirect jump is not known until run time.
b. The target instruction address of an indirect jump is known at the compile time.
c. The target of instruction of jal SUB is computed by the programmer.
d. jr ra is an indirect jump operation.

5. Which of the following is (are) true?
a. A computer fetches its first instruction from its hard disk.
b. Cache is pronounced as /keɪʃ/.
c. Cache is pronounced as /kætʃ/.
d. Cache is pronounced as /keɪtʃ/.

6. Which of the following is (are) true?
a. Virtual memory technique treats the main memory as a fully-set associative write-through cache.
b. Virtual address must be always larger than the physical address.
c. A TLB can be seen as the cache of a page table.
d. If an instruction TLB miss occurs, an instruction page fault is signaled.

7. Which of the following is (are) true?
a. When a cache write miss occurs, the written data are only updated in the main memory. This is the write-around policy.
b. There is no cache coherency problem for the write-through cache since the data are written into the next level of memory.
c. When a cache write hit occurs, the written data are only updated in the cache. This is the write-back policy.
d. Cache data inconsistency appears in a write-back cache when an I/O master writes data into the memory block which is cached.

8. Registers in a processor are typically synthesized from D-FFs.
a. Show the schematic of a gated D-latch based on S-R latch. 10%
b. Use the gated D-latch above to construct a D flip-flop. 10%
c. Show a 4-bit register based on the above D flip-flop. 10%