編號： 186

國立成功大學 104 學年度碩士班招生考試試題

系所組別：電機工程學系丁、戊組

考試科目：計算機組織

考試日期：0211，節次：2

※ 考生請注意：本試題不可使用計算機。 請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

Choose the correct answers for the following multiple choice problems. Each question may have more than one answer. 10 points each, no partial point, no penalty.

1. Which of the following statements is (are) true for data alignment?
   (a) For a word size of 4 bytes, this 32-bit address, 0xF0ABCCC is aligned.
   (b) For a word size of 8 bytes, this 32-bit address, 0xF0ABCCC is aligned.
   (c) For a cache line size of 32 bytes, this 32-bit address, 0xF0ABCE0 is aligned.
   (d) For a page size of 8KB, this 32-bit address, 0xF0ABC00 is aligned.

2. Which of the following statements is (are) true for virtual memory system?
   (a) The flash memory is a volatile device and it can be used for the swap space.
   (b) The operating system usually creates the space on flash memory or disk for all the pages of a process when it creates the process.
   (c) The space on the disk or flash memory reserved for the full virtual memory space of a process is called swap space.
   (d) A memory access violation can be detected by the memory management unit.

3. For a conditional branch instruction such as beq rs, rt, loop, which of the following statements are true?
   (a) The label "loop" defines the base address of the branch target.
   (b) The label "loop" is an offset relative to the program counter which points to the next sequential instruction of the branch instruction.
   (c) The label "loop" is an unsigned number.
   (d) The label "loop" is coded into the instruction as "loop".

4. Which of the following statements is (are) true for virtualization?
   (a) The software that supports virtual machine is called a virtual machine monitor (VMM) which determines how to map the virtual resources to the physical resources.
   (b) The cost of processor virtualization depends on the workload. User-level processor-bound programs often have zero virtualization overhead.
   (c) OS-intensive workloads which execute many system calls and privileged instructions can result in high virtualization overheads.
   (d) Virtualization is a simulation program that performs page walk for the virtual memory system.

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5. Which of the following is (are) true for cache system? The address is 32-bit long for each case.
   (a) A 64KB direct-mapped cache has a line size of 64 bytes. The tag width is 18 bits.
   (b) A 64KB direct-mapped cache has a line size of 64 bytes. The total tag memory is 16 Kbits.
   (c) A 64KB 4-way set associative cache has a line size of 64 bytes. The tag width is 16 bits.
   (d) A 64KB 4-way set associative cache has a line size of 64 bytes. The total tag memory is 18 Kbits.

6. Which of the following is (are) true for branch hazard in a pipelined processor?
   (a) Branch prediction can eliminate branch hazard completely.
   (b) Branch hazard comes from a data access hazard. It happens frequently.
   (c) A branch hazard arises from the need to make a decision based on the result of the branch instruction.
   (d) Branch hazard is a control hazard when the proper instruction cannot execute in the proper pipeline clock cycle because the instruction was fetched is not the one that is needed.

7. Which of the following is (are) true for processor implementation? Assume that for a single cycle implementation, the processor's cycle time is T nsec. The instruction count of the program to run is N.
   (a) For single cycle implementation, T is determined by the instruction which has the longest latency.
   (b) If N is the program instruction count, for single cycle CPU, it takes time of $N \times T$ nsec.
   (c) For multi-cycle implementation that uses one fifth of T for the CPU clock cycle time, the program execution time is 0.2 N × T nsec.
   (d) For a five-stage pipeline implementation that also uses 0.2T for the CPU clock cycle time, the program execution time is 0.2 N × T nsec.

8. Which of the following is (are) true about program performance?
   (a) The processor pipeline design affects the average cycles per instruction (CPI) and the clock cycle time which can be achieved.
   (b) Branch prediction improves the IPC, instruction per cycle of a pipelined processor.
   (c) The programming language affects the instructions count since the statements in the language are translated into the processor instructions.
   (d) The instruction set architecture affects the instruction count, clock rate, and CPI.

9. Using 8Kx8 SRAM chips for the memory system, which of the following is (are) true?
   (a) For 1 MB memory system, it needs 64 SRAM chips.
   (b) The 8Kx8 chip has 8K address pins.
   (c) It needs at least 8 chips for the connection to a 64-bit data bus for proper operation of full bus width access. So the minimum memory size is 64KB.
   (d) It needs at least 4 chips for the connection to a 64-bit data bus for proper operation of full bus width access. So the minimum memory size is 32KB.

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10. Which of the following is (are) true about cache operations?
    (a) A processor writes data into a cache line, which is also updated in other processor's cache. This is the write-through policy.
    (b) When a data cache write hit occurs, the written data are also updated in the next level of memory. This is the write-back policy.
    (c) When a data cache write miss occurs, the cache controller first fetches the missing block into cache and then the data are written into the cache. This is the write-allocate policy.
    (d) When a data cache write hit occurs, the data are only written into the cache. This is the write-back policy.