※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1.　Find the word or phrase from the list below that best matches the description in the following questions (1.1 to 1.10). Each answer should be used only once. (2 points each)

(a.) assembler　(b.) bit　(c.) binary number (d.) cache　(e.) CPU (f.) chip　(g.) compiler　(h.) control (i.) defect　(j.) DRAM　(k.) memory　(l.) operating system　(m.) semiconductor　(n.) supercomputer (o.) yield　(p.) die　(q.) loader　(r.) linker　(s.) SRAM　(t.) coverage (u.) procedure (v.) pipeline (w.) ISA.

1.1　Integrated circuit commonly used to construct main memory.

1.2　Location of programs when they are running, containing the data needed as well.

1.3　Microscopic flaw in a wafer.

1.4　Percentage of good dies from the total number of dies on the wafer.

1.5　Program that translates a symbolic version of an instruction into binary version.

1.6　Program that translates from a higher level notation to assembly language.

1.7　Small, fast memory that acts as a buffer for the main memory.

1.8　Substance that does not conduct electricity well.

1.9　Base 2 number.

1.10 Component of the processor that tells the datapath, memory, and I/O devices what to do according to the instructions of the program.

2.　Fill in the appropriate term or terminology for the underline fields: (6 points each)

(a)　move $s1, $zero =　add ____, ____, ____

(b)　CPU execution time = Instruction count x _____ x clock cycle time.

(c)　_____ is a technique in which data blocks needed in the future are brought into the cache early.

(d)　For a 64-bit data, if the least significant byte (B0) is stored at memory address 8N where N is an integer $\geq$ 0, this storage order is called _____ endian.

(e)　For a 64-bit data, if the least significant byte (B0) is stored at memory address 8N+3 where N is an integer $\geq$ 0, this storage order is called _____ endian.

Choose the correct answers for the following multiple choice problems. Each question may have more than one answer. 10 points each, no partial point, no penalty.

3.　Which of the following statements is (are) true for stack operations?

a.　Callee is a procedure that executes a series of stored instructions based on parameters provided by the caller and then returns control to the caller.

b.　Jal procedure_name, is the instruction that calls procedure_name and returns from the callee.

c.　Stack is a data structure for spilling registers organized as a last-in-first-out queue.

d.　Stack pointer, sp, is the register containing the address of program being executed.

e. Push operation can be achieved by executing a store instruction.

4. Which of the following statements is (are) true for IEEE 754 floating point representation?

   a. IEEE 754 standard defines the double precision number to be a 128-bit format.

   b. If a floating point number is shown in the form of $(-1)^S \times (1+F) \times 2^E$ where S defines the sign of the number, F the fraction field, and E the exponent, this means the leading 1-bit of normalized binary numbers is implicit.

   c. IEEE 754 binary representation of -0.75 (decimal number) is 10111111011000000000000000000000 for single precision.

   d. The floating point number represented in a biased exponent is actually this value: $(-1)^S \times (1+F) \times 2^{E-Bias}$

   e. Since there is no way to get 0.0 from this form: $(-1)^S \times (1+F) \times 2^{E-Bias}$, we will not be able to represent 0.0 in floating point format.

5. Which of the following is (are) true about memory management unit?

   a. A TLB miss can be handled either in software via privileged instructions or hardware state machine.

   b. A TLB miss invokes an operation called page walk which finds the missing entry from the page table.

   c. The instruction causing the TLB miss is a restartable instruction once the TLB miss is served.

   d. The faulting instruction of a page fault is not restartable.

   e. The TLB is a software cache for page table.

6. Which of the following is (are) true about virtual memory operations?

   a. The physical location of a page is managed by the linker.

   b. TLB is a cache for instruction and data.

   c. Page table is a data structure managed by the operating system.

   d. If a page fault occurs, this signals that the requested page is not in the main memory.

   e. A TLB miss also signals the occurrence of a page fault.

7. Which of the following is (are) true about cache coherence?

   a. There is no cache coherence issue for using a write-through cache since the written result is also updated in the next level of memory.

   b. There is no cache coherence issue for using a write-back cache since the written result is not updated in the next level of memory.

   c. If the I/O data are non-cacheable, then there is no cache coherence issues for I/O operations.

   d. The instruction cache has no cache coherence issue if self-modifying code is prohibited.

   e. To resolve cache coherence, one can use the write-through policy to enforce memory consistency.