※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. For a five-stage pipeline processor, answer the following questions: 5 points each.

   a. In the MIPS five stage pipeline, where is the earliest stage that can compute the branch outcome? Why?

   b. Can we find a possible branch target at the IF stage? How?

   c. In the pipelined datapath, which components should be connected to the CPU clock?

   d. If the control unit is located at the ID stage. How might the control unit affect the CPU clock?

   e. Is there a structure hazard of reading the source register operands at the ID stage and the write back of the destination register at the WB stage, why yes or why no?

2. In a five-stage pipelined processor, multiple exceptions may occur at the same clock cycle. Answer the following questions: 5 points each

   a. Which stage can detect an illegal instruction?

   b. What might be the possible causes that result in an illegal instruction?

   c. Which stage(s) can detect memory access violations?

   d. TLB exception may occur at which stage(s)?

   e. If multiple exceptions have occurred at the same time, which PC should be identified and saved for precise interrupt?

Choose the most appropriate answers for the following multiple choice problems. Each question may have more than one answer. 10 points each, no partial point, no penalty.

3. Using 16K x 8 SRAM modules for on-chip memory system, which of the following is (are) true?

   a. For 1 MB memory system, it needs 64 SRAM modules.

   b. The 16K x 8 module has 14 address lines.

   c. The 16Kx8 module has 16K address lines.

   d. It needs at least 8 modules for the connection to a 64-bit data bus. So the minimum memory size is 128KB.

   e. It needs at least 8 modules for the connection to a 64-bit data bus. So the minimum memory size is 64KB.

4. For a conditional branch instruction such as beq, rs, rt, foo, which of the following statements are true?

   a. The label "foo" defines the base address of the branch target.

   b. The label "foo" is an offset relative to the program counter which points to the next sequential instruction of the branch instruction.

   c. The label "foo" is translated into an unsigned number.

   d. The label "foo" is coded into the instruction as a string.

   e. The label "foo" is coded into the instruction as a signed number.

5. Which of the following is (are) true for the forwarding unit used in a typical five-stage pipelined processor?

    a. The forwarding unit is used to bypass the write-back result due to RAW hazards.

    b. The forwarding unit is used to forward data to the instruction cache.

    c. The forwarding unit compares the source register number of the instructions in the MEM and WB stages with the destination register numbers of the dependent instruction.

    d. The forwarding unit compares the destination register number of the instructions in the MEM and WB stages with the source register numbers of the dependent instruction.

    e. The forwarding unit is a combinational logic.

6. Which of the following statements is (are) true for virtual memory system?

    a. The space on the disk or flash memory reserved for the full virtual memory space of a process is called swap space.

    b. Virtual memory function can be enabled through software control.

    c. Virtual memory technique treats part of the main memory as a fully-set associative write-back cache for program execution.

    d. A translation lookaside buffer can be seen as the cache of a page table.

    e. A page table is shared among the programs in execution.

7. Which of the following statements is (are) true?

    a. Checking the state of an I/O device to see if it is time for the next I/O operation is called I/O polling.

    b. A multi-core system using a write-through cache as its private cache will prevent the cache coherence problem since the written data are also updated in the main memory.

    c. When an interrupt occurs, the processor always responds to the interrupt and enters the interrupt service routine. This is called an interrupt request.

    d. ISA (instruction set architecture) is an abstraction that enables different implementations of the same ISA for the processor, for example, a pipelined implementation or a non-pipelined one.

    e. Using a DMA controller to perform memory-to/from I/O operations is called CPU I/O.