編號： 178

國立成功大學108學年度碩士班招生考試試題

系　　所：電機工程學系

考試科目：計算機組織

考試日期：0223，節次：2

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

Choose the most appropriate answers for the following multiple choice problems. Each question may have more than one answer. 10 points each, no partial point, no penalty.

1. For the finite state machine implementation of a multi-cycle non-pipelined processor, which of the following is (are) true when the processor encounters an undefined instruction?
   (a) The undefined instruction is detected in the fetch cycle.
   (b) The undefined instruction is detected in the decode cycle.
   (c) The undefined instruction is executed as normal, but the result is discarded.
   (d) The undefined instruction causes an internal processor trap.
   (e) The undefined instruction is re-executed again.
2. For a 5-stage pipelined processor, which of the following is (are) true when the processor encounters an undefined instruction?
   (a) The undefined instruction goes through the pipeline as a no-op when detected.
   (b) The undefined instruction causes the pipeline to stall.
   (c) The processor stops several cycles and enters the undefined instruction exception.
   (d) The processor fetches the undefined instruction again.
   (e) The processor resets itself.
3. For a 5-stage pipelined processor, which of the following is (are) true when the processor encounters a data fault?
   (a) The processor enters a data fault exception.
   (b) The processor also enters an instruction exception.
   (c) The data fault is signaled by the MMU unit.
   (d) The data fault is caused by the execution of a load or store type instruction.
   (e) The data fault is caused due to the incorrect data of an arithmetic instruction.
4. About processor execution model, which of the following is (are) true?
   (a) A vector arithmetic instruction can be executed in the form of SIMD operation.
   (b) An SIMD arithmetic instruction has multiple data operands which are for the same intended operation.
   (c) A multi-core processor usually runs in the form of MIMD.
   (d) A GPGPU usually runs in the form of SIMT.
   (e) SIMT stands for single instruction multiple threading.
5. Which of the following is (are) true about data cache?
   (a) When a data cache write miss occurs, the cache controller first fetches the missing block into the cache and then the data are written into the cache. This is the write-allocate policy.
   (b) When a data cache write hit occurs, the data are only written into the cache. This is the write-back policy.
   (c) Data cache is typically deployed at the fetch stage of a pipelined processor.

(d) A L1 data cache is typically unified with the L1 instruction cache to reduce cache size.
(e) A write buffer is typically deployed with the data cache to improve performance.

6. About cache coherency, which of the following is (are) true?
(a) There is no cache coherency issue for a write-through cache since data are also written in the next level memory system.
(b) Cache coherency only occurs in multi-core processor system.
(c) Cache coherency only occurs in write-back cache.
(d) There is no cache coherency issue about an instruction cache since it is typically read-only.
(e) There is no cache coherence issue in a single processor cache system.

7. In MIPS, " beq r1, r2, L1" is a conditional branch, in ARM's assembly, this is done by cmp r1, r2, followed by a beq L1 like operation. Which of the following is (are) true?
(a) cmp sets the comparison result in register r2.
(b) In MIPS, comparison of r1 and r2, and branch to L1 are performed in the same instruction.
(c) cmp sets the comparison result in a condition code register.
(d) beq L1 compares r1 and r2.
(e) cmp performs JUMP to L1 conditionally.

8. Which of the following instructions can be used to implement A = A + B?
(a) ADD A, B, B
(b) ADD A, B
(c) ADD A, A, B
(d) ADD A, B, A
(e) ADD B, A, B

9. Which of the following are true?
(a) Checking the status bit of an I/O address to see if it is time for the next I/O operation is called interrupt.
(b) When an interrupt occurs, the processor always responds to the interrupt and enters the interrupt service routine.
(c) ISA (instruction set architecture) is an abstraction that enables different implementations of the same ISA for the processor.
(d) A page fault is signaled by a system call.
(e) RISC-V is an ISA specification.

10. About I/O and DMA operations, which of the following is (are) true?
(a) Programmed I/O is performed by the processor which executes the I/O programs.
(b) When I/O devices are mapped onto the memory space, this is called memory-mapped I/O.
(c) A DMA controller executes software for memory accesses.
(d) A DMA controller performs I/O operations by itself.
(e) DMA is short for Data Memory Access.