國立成功大學

110學年度碩士班招生考試試題

編　號：177

系　所：電機工程學系

科　目：計算機組織

日　期：0202

節　次：第 2 節

備　註：不可使用計算機

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※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Design an instruction TLB (ITLB), data TLB (DTLB), and data cache respectively for a 5-stage pipeline processor. Assume that both the virtual address and physical address are 32 bits. The page size is 8KB. The ITLB has 32 entries with fully set associativity. The DTLB is direct-mapped; has 64 entries. The data cache is physically addressed; cache size is 32KB, 4-way set associative, line size 32 bytes.
   a. Show the ITLB block diagram going from a virtual address to the output of a physical page number. Clearly show the width of the tag and data fields. 10 pts.
   b. Show the DTLB and data cache block diagram going from a virtual address, to DTLB, and output of the physical address, which then is used to access the data cache. 10 pts.
   c. Show how to connect the two TLBs and data cache to the pipeline. Clearly show what address is used to look up the TLBs. 10 pts

2. To implement a "swap rs1, rs2" instruction (Reg[rs2] = Reg[rs1]; Reg[rs1] = Reg[rs2]), answer the following questions:
   (a). How many register writes are required in the same cycle?　5 pts
   (b). Draw a n-bit register file circuit showing the implementation of two read ports. 5 pts.

3. A virtual memory system has the following parameters: virtual address 39 bits, physical DRAM installed 32 GB, page size 8KB, page table entry size 8 bytes. Answer the following questions:
   (a). For a single-level page table, how many page table entries (PTEs) are needed? 5pts.
   (b). How much physical memory is needed for storing the page table? 5pts.

4. Briefly explain the following terminology related to pipeline operation.
   (a) Data hazard (Use a two-instruction sequence to explain.) 5pts
   (b) Structure hazard. 5pts
   (c) Load-use data hazard. 5pts
   (d) Control hazard or branch hazard. 5pts.
   (e) Pipeline stall. 5pts.

5. Define or explain the following terminology.
   (a) Programmer visible register. 5 pts
   (b) Instruction set architecture (ISA). 5 pts
   (c) Abstraction. 5 pts
   (d) Single instruction stream, multiple data streams (SIMD). 5 pts
   (e) Atomic operation. 5pts