國立成功大學

111學年度碩士班招生考試試題

編　號：177

系　所：電機工程學系

科　目：計算機組織

日　期：0219

節　次：第 2 節

備　註：不可使用計算機

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※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Which of the following statement about program execution is/are TRUE? (10pts, no partial point, no penalty)
   (a) CPI stands for **C**lock **P**eriod/**I**nstruction.
   (b) IPC stands for **I**nstruction **p**er **C**ycle.
   (c) CPU time is the overall time that CPU spends on computing for a specific task with operation system and other task running.
   (d) Assuming computer A runs a program in 10 seconds, and computer B spend 50% less time than computer A running the same program. Computer B is 1.5 times faster than computer A.

2. Compile the following C code to RISC-V or MIPS instructions. (10pts)
   $$f = a + (b + (c + d))$$
   Please specify your assumption and write down comments on each instructions.

3. During a procedure call, which of the following is/are preserved? (10pts, no partial point, no penalty)
   (a) Saved registers
   (b) Temporary registers
   (c) Stacks below the stack pointer
   (d) Stack above the stack pointer
   (e) Stack pointer

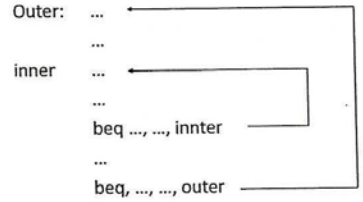
4. About IEEE754 standard floating-point, which of the following is/are TRUE? (10pts, no partial point, no penalty)
   (a) Floating point representation consist of only three part, sign, exponent and fraction.
   (b) Use 2's complement on both exponent and fraction representation
   (c) IEEE754 preserve encodings for" Infinity", "NaN". However, it fails to represent "denormalized numbers".
   (d) The precision of floating-point is relative precision depending on the exponent part of floating-point.

5. Pipeline is an implementation technique in which multiple instructions are overlapped in execution. Which of the following is/are TRUE? (10pts, no partial point, no penalty)
   (a) Pipeline can speed up overall performance due to latency of each instruction is improved
   (b) Pipeline bubble reduces overall speedup
   (c) For an N stage ideal pipeline, the best throughput is N IPC.
   (d) Pipeline speed is limited by the fastest stage.

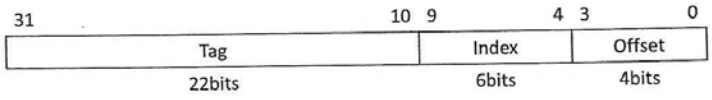
6. Different cache design in memory hierarchies may come with positive and negative effect. Which of the following is/are TRUE? (10pts, no partial point, no penalty)
   (a) Increase cache size may decrease capacity misses.
   (b) Increase associativity may increase miss rate due to conflict misses.
   (c) Assuming cache size is fixed, very large block size could increase miss rate.
   (d) Assuming cache size is fixed, very large block size could decrease miss rate.

7. There are three different type of pipeline hazard. Write down their name and cause. (10pts)

8. Dynamic branch prediction is a technique to predict branch taken or not at runtime. Assuming a processor use simple 1-bit prediction scheme on each branch while executing the following instructions. Please write down when and why mispredictions happen. (10pts)



9. Assuming a direct-mapped cache is accessed by the following bits of address. (10pts)



   What is the cache block size (in words)?
   How many blocks does the cache have?

10. Describe the difference, pros and cons of "Fine-grained multithreading" and "Coarse-grained multithreading". (10pts)