國立成功大學

112學年度碩士班招生考試試題

編　號：180

系　所：電機工程學系

科　目：計算機組織

日　期：0206

節　次：第 2 節

備　註：不可使用計算機

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※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. (10pts, no partial point, no penalty) Consider a pipelined RISC-V/MIPS processor. Which of the following statement is/are TRUE?
   (a) If input of a subsequent instruction has some dependences on output of previous instruction, this is called structure hazard.
   (b) ID stages is for registers fetch and instruction decode.
   (c) IF stage use only instruction memory, no data memory access required.
   (d) If we are designing a processor that can only execute R-type instruction, only 4 stages (IF, ID, EXE, MEM) are needed to be implemented.

2. (10pts, no partial point, no penalty) Pipelining is an implementation technique in which multiple instructions are overlapped in execution. Which of the following statement about pipeline is/are TRUE?
   (a) The clock rate of a pipelined hardware is determined by the fastest stage.
   (b) The speedup of pipelining comes from shorter clock period, which results in smaller overall delay.
   (c) Since the shortest delay determines clock period, we can split the acyclic combinational logic of critical path into two parts for faster clock period.
   (d) In a 5-stage pipelined RISC-V/MIPS CPU, hardware resources can be shared across different stages.

3. (10pts, no partial point, no penalty) Parallelism is a technique to enhance performance. Which of the following statement about parallelism is/are TRUE?
   (a) Since course-grained multithreading switches threads only on expensive stalls, it is limited in its ability to overcome throughput losses.
   (b) Simultaneous multithreading (SMT) is a variation on hardware multithreading that uses the resources of multiple single-issue, dynamically scheduled pipelined processor.
   (c) MIMD is more energy efficient than SIMD, since MIMD can process multiple instruction at same time.
   (d) Instruction pipeline with Out-of-order execution or superscalar execution can be regarded as Instruction Level Parallelism (ILP)

4. (10pts, no partial point, no penalty) Which of the following statement is/are TRUE? (10pts, no partial point, no penalty)
   (a) CPU time is total time spent processing on a given job, including I/O time.
   (b) In the IC design flow, the gate level implementation is the abstraction of the transistor level circuit
   (c) Since CPI represents the average of how many cycles for a processor to execute an instruction, we can evaluate the performance of two CPUs by comparing the CPI when running the same program (compiled separately).
   (d) Most tablet and smart phone use resistive touchscreen, since it allows multiple touches simultaneously

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5. (10pts, no partial point, no penalty) Which of the following statement about RISC-V/MIPS instructions is/are TRUE? (10pts, no partial point, no penalty)
   (a) Arithmetic instructions operands can be registers or memories.
   (b) Stack pointer is a value denoting the most recently allocated address in a stack that shows where registers should be spilled or where old register values can be found.
   (c) Programs are stored in memory to be read or written, but in a special format called machine sector, which is different from normal data stored in memory.
   (d) A basic block is a sequence of instructions without branches.

6. (10pts, no partial point, no penalty) Which of the following statement about cache is/are TRUE? (10pts, no partial point, no penalty)
   (a) Cache relies on the principle of locality to try to find the desired data in the higher levels of the memory hierarchy, which is different from the big idea of prediction.
   (b) In a direct mapped cache, each memory location is mapped directly to two specific locations in the cache.
   (c) A set associative cache reduces cache misses by more flexible placement of blocks.
   (d) If the total cache size is kept the same, increasing the associativity raises the number of blocks per set, which is the number of simultaneous compares needed to perform the search in parallel.

7. (10pts) Assume we use a processor with 2 GHz clock rate to run a program which requires the following executions.

Instruction Type	# of instructions	CPI
FP instructions	40×10^6	2
INT instructions	40×10^6	1
Load/Store instructions	30×10^6	5
branch instructions	20×10^6	5

   By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

8. (10pts) Using Booth's algorithm to do the following multiplication and answer the question.
   How many additions/subtractions needed to be computed?
   $0111\ 1110_2 \times 0111\ 1110$
   Number of additions = _____?
   Number of subtractions = _____?

9. (10pts) What's the value of *x5/$t1* after the following RISC-V/MIPS instructions? (in decimal)

----------RISC-V----------

x7 holds the value $0x0000000000011100_{hex}$.

```
        blt x7, x0, ELSE
        ori x5, x0, 8
        jal x0, DONE
ELSE:   ori x5, x0, 4
DONE:
```

----------MIPS----------

$t0 holds the value $0x0000000000011100_{hex}$.

```
        blt $t0, $zero, ELSE
        ori $t1, $zero, 8
        jal x0, DONE
ELSE:   ori $t1, $zero, 4
DONE:
```

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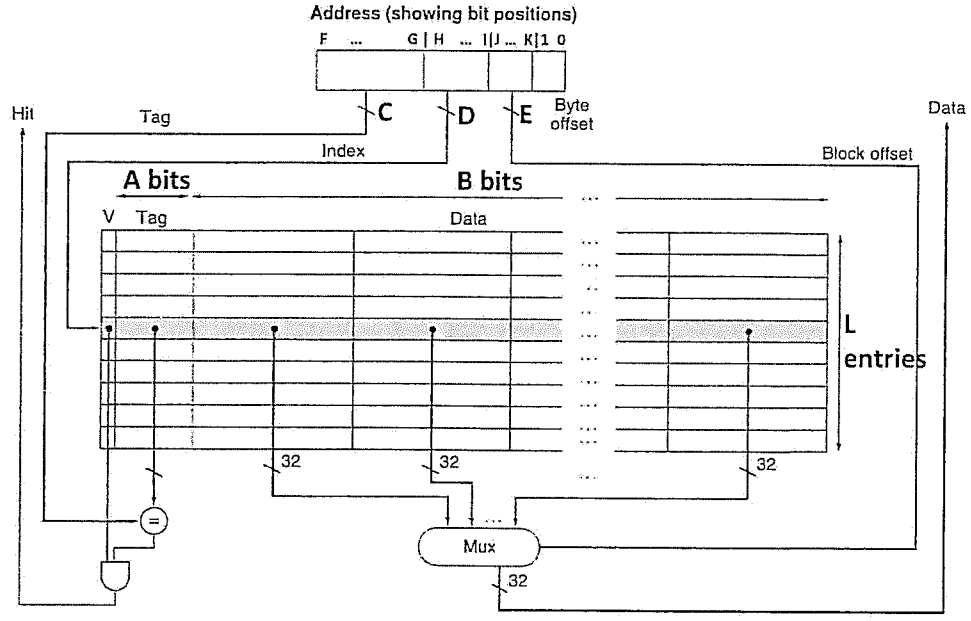
10. (10pts) Consider the following cache design with the following spec.

address size: 64 bits.

32 words of data in a line.

128 lines.



A~L are positive integers.

A=____, B=____, C=____, D=____, E=____, F=____,

G=____, H=____, I =____, J =____, K=____, L=____.

(-1 points for each incorrect answer)