國立成功大學

112學年度碩士班招生考試試題

編　號：174

系　所：電機工程學系

科　目：計算機組織與作業系統

日　期：0206

節　次：第 1 節

備　註：不可使用計算機

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※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. (10pts, no partial point, no penalty) Which of the following instructions should be privileged?
   a. Set value of timer.
   b. Read the clock.
   c. Clear memory.
   d. Issue a trap instruction.
   e. Turn off interrupts.
   f. Modify entries in device-status table.
   g. Switch from user to kernel mode.
   h. Access I/O device

2. (10pts, no partial point, no penalty) Which of the following statement about process is/are TRUE?
   (a) Context switch means switching the CPU core to another process, which requires performing a state save of the current process and a state restore of a different process.
   (b) A process terminates when it finishes executing its final statement and asks the operating system to delete it by using the exit() system call.
   (c) An empty process is a process that may be performing an activity but is not apparent to the user.
   (d) A visible process is the current process visible on the screen, representing the application the user is currently interacting with.

3. (10pts, no partial point, no penalty) Which of the following statement about I/O is/are TRUE?
   (a) Handshaking between the DMA controller and the device controller is performed via a pair of wires called DMA-request and DMA-acknowledge.
   (b) An interrupt is an unexpected event from within the processor, while exception is an unexpected event from outside the process.
   (c) Increase concurrency by using DMA-knowledgeable controllers or channels to offload simple data copying from the CPU can improve the efficiency of I/O.
   (d) When an application issues a non-blocking system call, the execution of the calling thread is suspended. The thread is moved from the operating system's run queue to a wait queue

4. (10pts, no partial point, no penalty) Pipeline hazards are situations that prevent starting the next instruction in the next cycle. Which of the following is/are TRUE?
   (a) For a datapath that uses separated memories for instruction and data, structure hazard still occurs when memory writing and instruction fetching are executed in the same cycle.
   (b) In RISC-V 5 pipeline design, making each instruction have the same number of stages is a way to reduce structure hazards.
   (c) Separating the register reading and writing process, which writes in the first half cycle and reads in the second half cycle, can reduce control hazards.
   (d) Control hazards could be reduced by moving branch address calculation to the IF stage.

5. (10pts, no partial point, no penalty) Virtual memory gives us the illusion of having more physical memory. Which of the following about virtual memory is/are TRUE?
   (a) Virtual memory uses main memory as a "cache" for secondary storage, which is usually managed by DRAM hardware.
   (b) Generally, virtual address space is smaller or equal to physical address space.
   (c) By using a larger TLB, the number of page faults and be reduced.
   (d) Virtual memory can provide protection for different tasks accessing the same physical memory by MMU

6. (10pts, no partial point, no penalty) Cache gives us an illusion of a large and fast memory. Which of the following statement about cache miss is/are TRUE?
   (a) Conflict misses occur low in direct mapped cache, and high in fully associative mapped cache.
   (b) Compulsory misses occur only in direct mapped and set associative caches
   (c) There is no way to reduce compulsory misses.
   (d) Fully associative caches have no conflict misses.

7. (10pts) Assume executing a program with a 2.0 GHz clock rate processor. The program consists of the following instructions.

Instruction type	Number of Inst.	Original CPI (Clock Per Instruction)	CPI reduction
FP instructions	70×10^6	1	50%
INT instructions	90×10^6	1	50%
L/S instructions	50×10^6	4	10%
branch instructions	8×10^6	2	10%

   (a) (5pts) How many seconds is the total execution time of the program (before improvement)?
   (b) (5pts) If we improve this machine by reducing its CPI and the reduction of each instruction is shown in the table. How many seconds is the execution time of the program?

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8. (10pts) Consider a computer system that has memory system including cache memory, main memory and disk. This computer system runs on an operating system that used virtual memory. Assuming the cache hit rate is 10% and main memory hit rate (after a cache miss) is 99%,

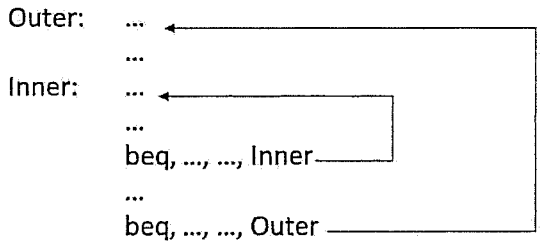
Operation	Access time
Access a word from cache	2ns
Access a word from RAM	10ns
Access a word from disk	10ms

What is the average time to access a word?

9. (5 pts) Please explain what is deadlock and what are the four necessary conditions for a deadlock situation.

(5 pts) Describe the difference between deadlock and starvation.

10. (10pts) Dynamic branch prediction is a technique to predict branch taken or not at runtime. Assuming a processor use simple 2-bit dynamic predictor on each branch while executing the following instructions.



(a) (5pts) Please draw the prediction scheme of 2-bit dynamic predictor.

(b) (5pts) Please write down when and why mispredictions happen.