國立成功大學

113學年度碩士班招生考試試題

編　號：177

系　所：電機工程學系

科　目：計算機組織

日　期：0201

節　次：第 2 節

備　註：不可使用計算機

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※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. (10pts, no partial point, no penalty) Consider a pipelined RISC-V processor. Which of the following statement is/are TRUE?
   (a) R-format instructions can operate on both register and memory.
   (b) I-format instructions do not directly operate on memories.
   (c) Argument and result registers should be preserved during procedure call.
   (d) Branch instruction use byte address to align with memory addressing.

2. (10pts, no partial point, no penalty) Which of the following statements about pipeline hazard is/are TRUE?
   (a) RAW hazards, also known as data hazards, occur when there is a dependency between the instruction in the instruction fetch stage and the instruction in the execute stage.
   (b) Control hazards, also known as branch hazards, arise when there is a mismatch between the predicted and actual outcomes of a branch instruction, leading to pipeline stalls.
   (c) Data dependencies are always resolved by forwarding, eliminating the possibility of data hazards in a pipeline.
   (d) Structural hazards result from resource conflicts, such as multiple instructions trying to use the same execution unit simultaneously.
   (e) WAW hazards, also known as write-after-write hazards, occur when two instructions attempt to write to the same register, causing conflicts in the writeback stage, which need to be serious considered in RISC-V pipeline.

3. (10pts, no partial point, no penalty) Virtual memory is a technique that uses main memory as a "cache" for secondary storage. Which of the following statement about virtual memory is/are TRUE?
   (a) In a system with virtual address and without Translation Look aside Buffer, every access to data by processor would require at least 2 memory references.
   (b) Virtual memory implements the translation of a program's address space to physical addresses.
   (c) A virtual memory block is called a page, and a virtual memory miss is called a page fault.
   (d) Write-through scheme, which ensuring that data are always consistent between the two memories, is suitable for virtual memory, since consistency between every process is the most critical consideration.

4. (10pts, no partial point, no penalty) Which of the following statement about Cache is/are TRUE?
   (a) In a write-through cache policy, data is written to both the cache and the main memory on every write operation.
   (b) Write-back caching can lead to a higher bus and memory bandwidth usage compared to write-through caching.
   (c) Write-back caching is generally more suitable for systems where write operations are frequent.
   (d) Write-back caching is more likely to experience consistency issues in a multi-processor environment.

5. (10pts, no partial point, no penalty) Which of the following statement about Multithreading is/are TRUE?
   (a) Multithreading involves the simultaneous execution of multiple threads within the same process.
   (b) In hardware multithreading, each thread has its own set of registers and program counter.
   (c) Context switching in multithreading refers to the process of switching between threads within the same process
   (d) Multithreading enhances parallelism by allowing multiple processes to run concurrently on a single processor

6. (10pts, no partial point, no penalty) Which of the following statement about addressing mode is/are TRUE?
   (a) Immediate addressing mode involves specifying the operand value directly in the instruction.
   (b) Register addressing mode utilizes an address stored in memory to access the operand.
   (c) Indirect addressing mode involves specifying the memory address directly in the instruction.
   (d) Indexed addressing mode uses an index register value to calculate the effective address.

7. (10pts, no partial point, no penalty) Compared to traditional CISC architectures, RISC-V generally achieves performance through:
   (a) Increased clock speed and pipelining complexity.
   (b) Efficient instruction execution with fewer clock cycles.
   (c) Extensive use of dedicated coprocessors and specialized instructions.
   (d) Frequent dependence on compiler optimizations for instruction decoding.

8. (10pts, no partial point, no penalty) Consider the following RISC-V assembly

```
addi x1, x0, 5
addi x2, x0, -5
addi x3, x0, 1

loop:
   beq x1, x0, endloop
   slli x4, x1, 2
   sub x1, x1, x3
   add x2, x2, x4
   j loop

endloop:
   sw x2, 4(x0)
```

What will be the final values of x2 after the program execution?

9. (10pts) A vector processor has a vector register length of 64 elements. It can perform a single vector addition operation in 5 clock cycles, regardless of the vector length. Given two vectors A and B, each containing 480 elements, calculate the total time it would take to perform element-wise addition of A and B using this vector processor.

10. (10pts) Consider a computer system with an associative cache. The cache has a total size of 32 KB, and each cache line can store 64 bytes of data. If the cache uses a 4-way set-associative mapping, calculate the following:
    (a) The number of sets in the cache.
    (b) The total number of cache lines in the cache.