1. (a) A silicon diode is in series with a 2-kΩ resistor and a 10-V power supply. Approximately what is the current in the circuit, if the diode is forward-biased?
   (b) If the measured diode drop is 0.6 V at 1 mA, obtain a more accurate value for the current in the circuit.
   (c) If the battery is reversed and if the diode breakdown voltage is 7 V, find the current in the circuit.
   (d) A second identical diode is added in series opposing (the two anodes are connected together). Approximately what is the current in the circuit?
   (e) The supply voltage in part (d) is reduced to 4 V, find the current in the circuit and the voltage across each diode. (15%)

2. (a) Sketch a two-input MOS (positive) NOR gate and verify that it satisfies the Boolean NOR equation.
   (b) Sketch a MOS R-S latch, and verify that if S=1 and R=0, a one is set into the memory.
   (c) Draw the circuit of MOS inverter with the enhancement load operating in the saturation region. Sketch the transfer characteristic if the load FET has a much higher resistance. What is the high value of the output voltage and the approximate value of the low output voltage.
   (d) Repeat part (c) for a load operating in the ohmic region.
   (e) Sketch the circuit of a transmission gate by using CMOS transistors. Explain the operation. (15%)

3. (a) Using Boolean algebra, verify that $\overline{\bar{A}+B}+\overline{\bar{A}+\bar{B}}=A$.
   (b) Indicate a block diagram of a 512×4-bit ROM, using two-dimensional addressing. Use a 64×32 matrix encoder.
   (c) Verify that a D-type FLIP-FLOP becomes a T-type if D is tied to $\bar{Q}$.
   (d) Draw a 1-MOSFET dynamic memory cell, and explain its operation briefly.
   (e) What is a stacked-gate memory cell? How is such a cell "programmed"? (15%)

4. An n-p-n silicon transistor with $\beta=50$ is used in the circuit of Fig. 1. (a) Find the quiescent point. The h parameters are $h_{fe}=50$ and $h_{ie}=1.1\ k\Omega$. Neglect all capacitive effects. Calculate (b) $A_I=-I_2/I_b$: (c) $R_i=V_b/I_b$: (d) $R_i'=V_b/I_1$: (e) $A_I'=-I_2/I_1$: (f) $A_V=V_o/V_b$: (g) $A_{VS}=V_o/V_s$: (h) P_o : (i) R_o'. (20%)

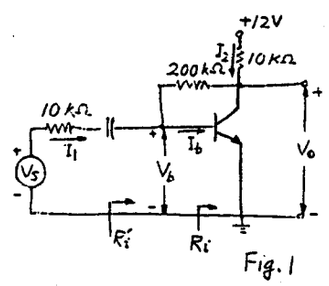

Fig. 1

5. (a) Draw the circuit of an OP AMP integrator and indicate how to apply the initial condition.
   (b) Design an integrator with an input resistance of 1 MΩ. Select the capacitor so that when $V_i=+10$ V, V_o travels from 0 to −10 V in 0.1 sec.
   (c) If $V_i=0$ and input offset voltage equals 5 mV, how long will it take for V_o to drift from 0 V to saturation? Explain how to eliminate this drift problem.
   (d) If $V_i=0$ and input bias current is 0.2 μA, how long will it take for V_o to drift from 0 V to saturation? Explain how to eliminate this drift problem if $I_{B1}=I_{B2}$.
   (e) If $I_{B1}\neq I_{B2}$, give the expression for V_o with the circuit modified as in part (d). (20%)

6. (a) For the feedback network shown in Fig. 2, find the transfer function V_f/V_o.
   (b) This network is used with an OP AMP to form an oscillator. Find the frequency of oscillation and the minimum amplifier gain.
   (c) Draw the network connected to the OP AMP to form oscillator. (15%)

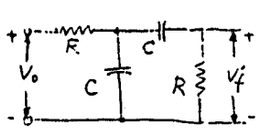

Fig. 2