1. Assume a machine with a vector-interrupt capability, where an I/O device supplies the starting address of the interrupt-service routine at the time the interrupt is acknowledged. Describe the sequence of events from the time the device requests an interrupt, until execution of the interrupt-service routine is started. (10%)

2. (a) What are the advantages and disadvantages of hardwired and microprogrammed control? (8%)
   (b) What are the relative merits of horizontal and vertical microinstruction formats? (6%)

3. In some computers, subroutine linkage is implemented in the following way. The calling subroutine instruction stores the return address into the first location of the subroutine,and then branches to the second location, where execution of the subroutine begins.
   (a) Define a suitable instruction for returning from the subroutine (4%)
   (b) Would the above linkage method support subroutine nesting? Why? (4%)
   (c) Would this linkage method support recursive calls (i.e. a subroutine call itself)? If not, illustrate a linkage method which can support recursive call. (5%)

4. "It is not possible to transfer data to a computer unless the computer is expecting arrival of such data." Comment on the validity of this statement by considering the following three possibilities for input operations.
   (a) Status checking (3%)
   (b) Interrupts (3%)
   (c) Direct memory access (3%)

5. Explain the following terminologies (15%)
   (a) Cache memory
   (b) Memory access time
   (c) Local area network
   (d) Dumb terminal
   (f) Bit slice

6. Compare the isolated I/O with Memory-Mapped I/O and illustrate two commercial processors which support only memory-mapped I/O. (12%)

7. For an one-bit binary subtractor (12%)
   (a) Find the simplified output functions of this circuit
   (b) Design this circuit with a decoder and external gates
   (c) Use PLA to implement this circuit
   (d) Use a ROM to implement this circuit

8. Use RS flip-flops to design a counter which counts in the Gray code sequence, 000,001,011,010,110,111,101,100 and repeat.
   (a) Derive the input equations for each flip-flop (12%)
   (b) Draw the logic circuit of this counter (3%)