(戊)

國立成功大學 79學年度電機研究所考試(計算機組織試題) 共 2 頁 第 1 頁

1. Explain the following terminologies. (15%)
   (a) Vector Computation.
   (b) Fault-Telerant system.
   (c) Virtural memory.
   (d) privileged Instructions.
   (e). RISC.

2. If the time-shared bus is used to Constructing a multiprocessor system. (15%)
   (a). Describe the bus structure of the time-shared bus.
   (b). Discuss the features it must provided in a multiprocessor configuration.
   (c). Compared to other approaches, discuss it's advantages and disadvantageand explain how to improve the drawback.

3. (a). Describe a Cache/Main memory structure which use the Set-Associate Mapping function.
   (b). Explain the Replacement algorithms which is used when a new block is brought into the Cache.
   (c). Discuss the Write-policies it is used to update the main memory. (15%)

4. Three techniques are possible for I/o operations. For each I/o method, discuss the hardware structure about the CPU and the I/O Interface, the procedure it needed to perform. and the overhead of the Software programming. (15%)

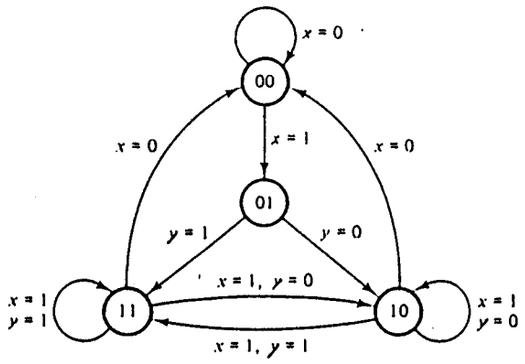
078

國立成功大學 79學年度碩博士班研究所 考試(計算機組織 試題) 共 2 頁 第 2 頁

5. A sequential circuit has four states and two input, x and y. The state diagram is shown in Fig. 1. (20%)

(a). Design the circuit with JK-FF. (use A.B.C as the FF's name).

(b). Use a 3-bits register and a ROM to implement this circuit.



Figure

6. A Booth's algorithm for 2's-Complement multiplication is shown in Fig. 2. (20%)

(a). Use (7)×(3), (-7)×(3), (9)×(-5), (-9)×(-5) as the example to perform the Booth's Algorithm.

(b). Draw the equivalent ASM chart, and the state table of this multiplier's Control Circuit.

(c). Use D flip-flop and a decoder to implement the circuit.

(d). Use One flip-flop per state method to implement this circuit.

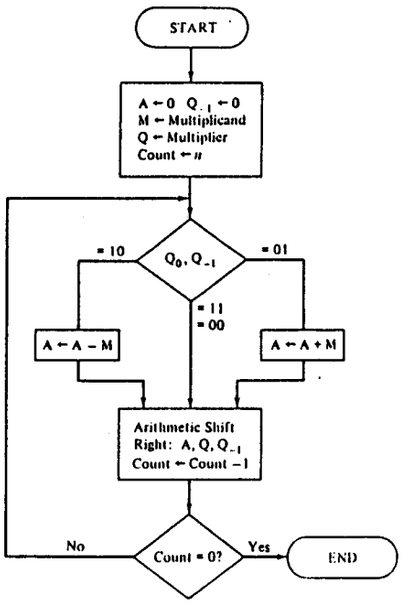


FIGURE Booth's algorithm for 2's-complement multiplication.

079