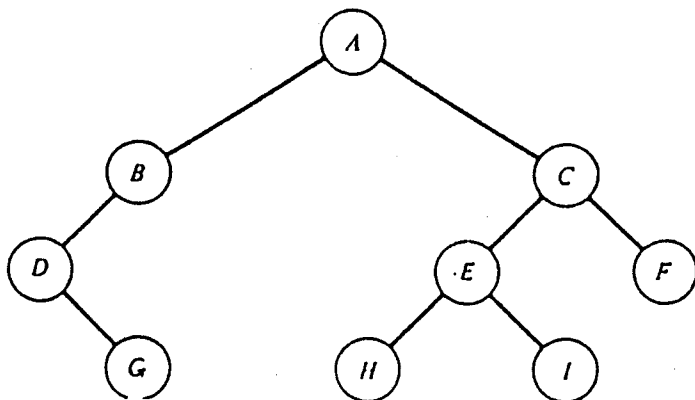
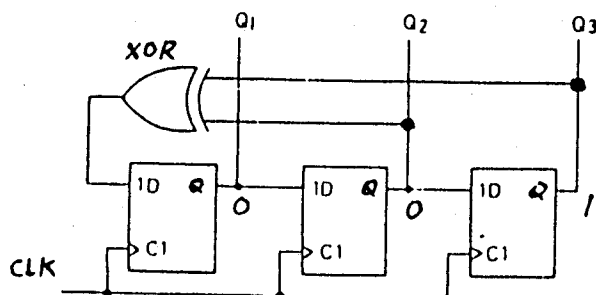


The total score is 100. The number in a pair of parentheses indicates the score of the corresponding question.

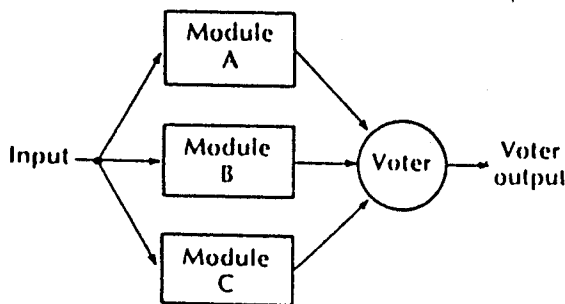
1. (20) Explain the following terms.
 - (a) (2) Priority queue
 - (b) (2) Hash collision
 - (c) (3) Descending heap
 - (d) (3) Transitive closure
 - (e) (2) Isolated I/O
 - (f) (2) Memory thrashing
 - (g) (3) Essential prime implicant
 - (h) (3) Field programmable gate array (FPGA)
2. (6) Write down the traversals of the following binary tree using *inorder*, *preorder*, and *postorder*.



3. (9) Write an algorithm to determine whether a directed graph is acyclic or not.
4. (10) Discuss the worst-case and average time complexities of the quicksort algorithm.
5. (10) Use the C language to write a push function and a pop function for a stack represented by a circular list. Clearly define the data structure and any function you use.
6. (15) For the following circuit, if the initial state of the register is $S_0 = 001$ as indicated in the figure, then the next state of this register will be $S_1 = 100$, followed by $S_2 = 010$, and so on.
 - (a) (5) Determine the period of this circuit when $S_0 = 001$, i.e., determine the smallest positive integer n such that $S_n = S_0 = 001$.
 - (b) (10) Clearly if $S_0 = 000$, then $S_1 = S_2 = \dots = 000$. Can you modify this circuit by adding some logic such that the period of this circuit becomes $2^3 = 8$ no matter what the initial state is?



7. (15) The following diagram is a triple modular redundant (TMR) system in which the functions of the three modules are the same and if two or more modules function correctly, the voter will give correct result. Assume the three modules are mutually independent and each module has a probability of p to function correctly.
- (5) Derive a formula for the probability that the voter will give correct result.
 - (5) Substitute $p = 0.4$, $p = 0.6$ and $p = 0.9$ into the formula you derived in (a) to obtain the exact values.
 - (5) Based on (b) what can you say about the reliabilities of a TMR system and a single module system? Discuss which is more reliable under various p .



8. (15) The following figure shows the timing diagram of a sequence of instructions using no pipelining, where I, E, and D represent *instruction fetch*, *execute*, and *transfer between memory and register*, respectively, A, B, C are three registers, and M and X denote some memory locations. For the following questions you may insert any desired wait states in any instruction and use NOOP (no operation) at any place.
- (5) Assume the memory is single-port accessible. Give a two-way pipelined timing diagram for the same sequence of instructions. Determine the speed-up, i.e., the ratio of clock cycles required for no pipeline and two-way pipeline structures.
 - (5) Similar to (a), but assume two memory accesses are allowed per phase and use three-way pipelines.
 - (5) Does the three-way pipeline structure achieve the best possible speed-up for this sequence of instructions? Justify your answer.

