1. To measure the processor performance, let us assume
   F = clock rate in MHz of the "input clock" to the CPU
   CPI = average clock cycles per instruction
   NI = number of instructions executed for a task

   a) write a formula representing the "processor performance" in MIPS (million instructions per second).
   b) write a formula representing the "processor performance" in processor time per task (which is the time the CPU is busy computing for this task, not including the time it waits for I/O) (10%)

2. Increasing the input clock frequency will improve the speed of the microprocessor. List at least 3 other characteristics which will also improve the speed of the microprocessor. (8%)

3. The segmentation organization has a number of advantages to the programmer over a nonsegmented address space. Describe these advantages. (8%)

4. Suggest reasons why RAMs are often organized with only one bit per chip, whereas ROMs are usually organized with multiple bits per chip. (10%)

5. Assuming equivalent refill-line (the group a cache loads when the CPU references any element of the group) size, why does a direct-mapped cache allow the fastest access, and why does a fully associative cache have the highest hit rate? (10%)

6. Describe and compare the following three kinds of buses:
   a) local buses (e.g. Vesa Local Bus)
   b) system buses (e.g. AT Bus)
   c) I/O buses (e.g. SCSI Bus) (12%)

7. In the implementation of a demand-paged virtual-memory system, 0.2% of the memory references will result in a page fault. The access time of main memory is 200ns, the time to copy a page to or from external memory is 20 ms, and the time to run the page-replacement algorithm is 1 ms. Estimate the effective cycle time of the main memory. State clearly ant assumptions you make in doing your calculations. (10%)

8. Using NAND gates to implement SL latch with control input. (10%)
   The function table is

C	S	R	Next state of Q
0	x	x	No change
1	0	0	No change
1	0	1	Q = 0; reset state
1	1	0	Q = 1; set state
1	1	1	Nondeterminite

9. Design a sequential circuit with JK flip-flops to satisfy the following state equations:
   A(t+1) = A'B'CD+A'B'C+ACD+AC'D'
   B(t+1) = A'C+CD'+A'BC'
   C(t+1) = B
   D(t+1) = D' (12%)

10. A simple CPU has four major phases to its instruction cycle: fetch, indirect, execute, and interrupt. Two 1-bit flags designate the current phase in a hardwired implementation.
    a) Why are these flags needed
    b) Why are they not needed in a microprogrammed control unit. (10%)