1. A long **cache line** is more useful for an instruction cache than for a data or mixed instruction and data cache. Is that right? Explain your answer. (10%)

2. What is the difference between the **vectored interrupt** and **nonvectored interrupt**. Describe how microcomputer's circuitry to handle vectored interrupt. (12%)

3. Describe the key differences between a **subroutine call** and a **trap**. (8%)

4. The typical small (PC-size) memory systems can be accessed in about 200ns. How would adding a cache affect the performance of a 4.77 Mhz PC? How might it affect the performance of a 20 or 33 MHZ 386- or 486-based PC? (12%)

5. A dynamic RAM must be given a **refresh cycle** 64 times per ms. Each refresh operation requires 150 ns and a memory cycle requires 250 ns. What percentage of the memory's total operating time must be given to memory refreshes? (8%)

6. A **bus cycle** corresponds to the time needed to do a data transfer between the processor and the addressed slave device. In the 32-bit Microprocessors, e.g. Intel 80386 or 80486, it might take more than one bus cycle to get a consecutive 4 byte data from memory. Explain why. (List all the possible reasons) (12%)

7. In some computers, why is it necessary to invalid the process cache when a new process is activated? (10%)

8. Compare the superscalar and superpipelined microprocessors. (8%)

9. (1) Using J-K flip-flops to design a **synchronous sequential counter** that counts the following sequence: (7%)

   000, 100, 101, 110, 111, 001, 000 ....

   (2) Is there any limitation in the clock rate in your design.(3%)

10. Given F=AB'D + A'B + A'C + CD
    (1) use a Karnaugh map to find the maxterm expression for F (3%)
    (2) use a Karnaugh map to find the minimum sum-of-product form for F' (3%)
    (3) Find the minimum product of sums for F (4%)