1. (1) Design a two bit adder and write down its truth table.
   (2) Use the Karnaugh Map to get the minimum forms of the combination circuit functions.(10%)

2. Design a Mealy network (using D flip-flops) that will examine a string of 0's and 1's applied to the X input of the network and generate an output Z=1 only when the 101 pattern occurs. (a) draw a state diagram (b) write the state transition table (c)design the Mealy network (10%).

3. What are the characteristics of RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer)? What are their advantages and disadvantages?(10%)

4. What is cache memory? Describe the advantages and disadvantages of three different cache mappings (1) direct mapping (2) associative mapping and (3) set-associative mapping. How can the cache memory improve the performance of a multiprocessor system with a common system bus? (15%)

5. Does a digital computer system need a clock? What is going to happen if there is no clock in a digital computer system? (5%)

6. The following sequence of virtual page numbers is encountered in the course of execution on a computer with virtual memory:
   3 4 2 6 4 7 1 3 2 6 3 5 1 2 3.
   Assume that a least-recently-used page replacement policy is adopted. Plot a graph of page hit ratio (fraction of page references in which the page is in main memory) as a function of main-memory page capacity n for $1 \le n \le 8$. Assume that main memory is initially empty.(10%)

7. Assume that a system is designed to have 16 address lines (A0-A15). Further assume that it is designed to have 4K of I/O space and the Memory is installed to its allowed maximum. What would be the sizes of memory in memory mapped I/O and isolated I/O design? What instructions would be required to access an I/O port, say at address 40, in both design?(10%)

8. How many times does the CPU need to refer to memory when it fetches and executes an indirect-address-mode instruction if the instruction is (a) a computation requiring a single operand; (b) a branch? In your answer please also specify the purpose of each memory access.(10%)

9. What is the relationship between a memory port controller and a bus controller? Show how to connect several devices to one memory system using a single system bus. How if several devices attempt to use the system bus simultaneously?(10%)

10. A RISC computer is normally approached by a load-and-store architecture. Is the declaration true or false? (10%)
    Give your reasons.