1. Why the microprocessors using ***synchronous bus***; such as Intel 80x86 CPU, can adapt to the fast and slow memory, i.e. they can use either high speed or low speed memory. (10%)

2. Why the access time of **SRAM** is short than that of **DRAM**. Illustrate at least two reasons. (10%)

3. Can you design isolated I/O for Motorola 680x0-based system? Why? (10%)

4. Why most virtual memory schemes make use of a translation lookaside buffer (TLB). (10%)

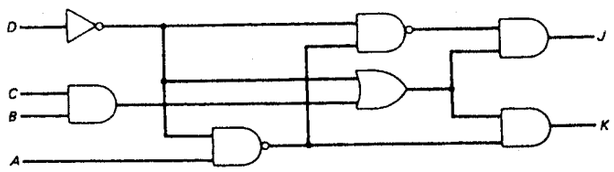
5. List the advantages and disadvantages of the shared memory multiprocessor systems and the distributed memory multiprocessor systems. (10%).

6. One way of speeding up read accesses in a memory system with a cache is to start reading the data from main memory in parallel with reading it from cache. If the requested datum is in cache, the value from main memory is then ignored. What are the advantages of this system? If the cache hit rate is 95% and is 10 times faster than main memory, how much gain is there, in terms of the percentage of memory access time being reduced, by using this simultaneous read? (Assume the simultaneous read reduces the access time to main memory by 20%.) (10%)

7. Describe two special machine instructions that a computer with masked and prioritized interrupts would need. (10%)

8. (a) Please list three ways for passing parameters and storing return address in a function call.
(b) For allowing the implementation of recursive function call, which method(s) should be used? Why? (10%)

9. Obtain the truth table for the circuit shown in the following figure. Draw an equivalent circuit for F with the minimal NAND gates. (10%)



10. Explain how the superscalar machines achieve greater performance. (10%)