1.(a) For the circuit shown in Fig. 1(a), assume Q_1 and Q_2 are identical (with a finite Early voltage V_A) and were biased in the forward active region. find the voltage gain $A_v(=v_o/v_i)$ for the cases of $R_L=\infty$ and $R_L\neq\infty$, respectively. (12%)

(b) Calculate the values of f_p (the dominant pole) and GBP (gain-bandwidth product) for the circuit shown in Fig. 1(b). Assume that $g_m=10mS$, $r_o=70k\Omega$, $R_D=10k\Omega$, $R_G=10k\Omega$, $C_{gs}=6pF$, and $C_{gd}=2pF$. The effect of C_{ds} can be neglected. (8%)

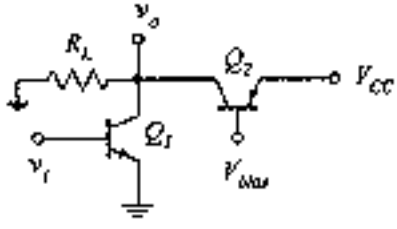

Fig. 1(a)

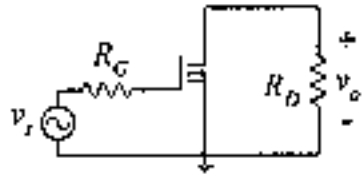

Fig. 1(b)

2.(a) A p-n junction at 300K with doping concentration of $N_a=10^{18}cm^{-3}$ in p-side and $N_d=10^{15}cm^{-3}$ in n-side, if n_i=1.5 x$10^{10}cm^{-3}$, what is the built-in voltage V_{bi}? If $C_{jo}=0.5pF$, please find the junction capacitance C_j when a reverse bias of $V_R=1V$ and 5 V is applied to the junction(4%)

(b) For the Zener diode circuit shown in Fig.2(a), the Zener breakdown voltage is V_Z=5.6 V and r_z=0. If the input voltage $v_i(t)=10\sin(\omega t)$ volt, please plot the transfer curve v_o as a function of v_i, also plot the waveform of $v_o(t)$ and $I_z(t)$.(6%)

(c) For the common-collector amplifier circuit shown in Fig.2(b), the signal source is directly coupled to the transistor base. If the dc component of v_s is zero, find the dc emitter current. Assume β=120, neglecting r_o, find R_i, the voltage gain v_o/v_s, the current gain i_o/i_i and the output resistance R_o?(8%)

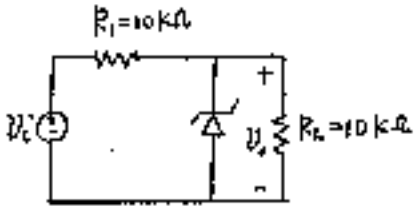

Fig. 2(a)

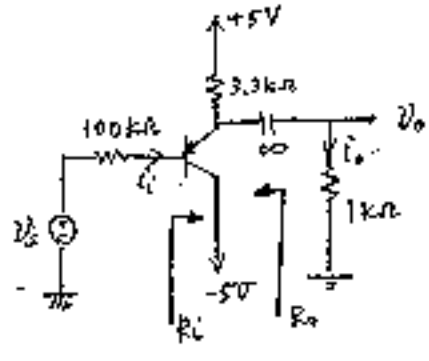

Fig. 2(b)

3.(a) What is the function realized by the dynamic logic circuit shown in Fig.3(a)?(5%)

3.(b) Both of the TTL gate tied together as shown in Fig.3(b), the transistors are identical and have β_F=25 and β_R=0.5.
(i) Determine β_{Fmin} for proper operation. Assume that Q_3 and Q_5 saturate for v_s=V(1).(7%)
(ii)What is the fan-out?(8%)

(背面仍有題目,請繼續作答)

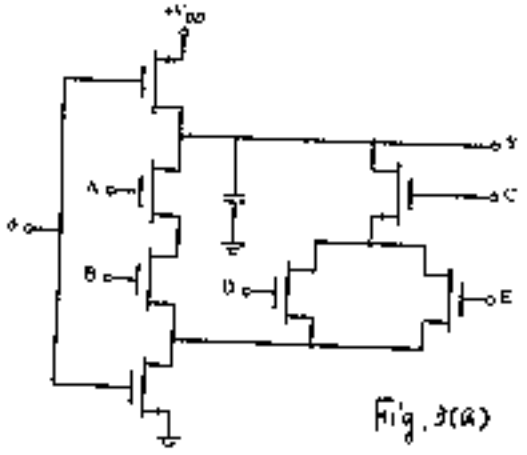

Fig. 3(a)

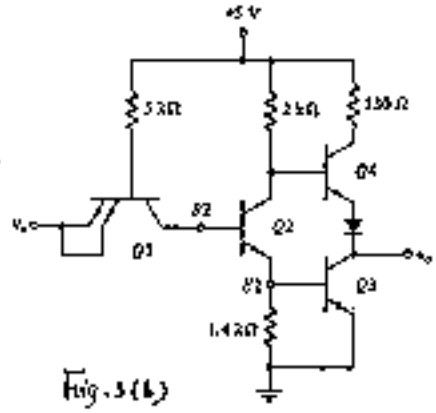

Fig. 3(b)

4.(a) Show how a 2 MHz switched-capacitor(SC) circuit behaves as a resistor of 50kΩ.(10%)

(b) Draw two stray-insensitive integrators.(10%)

5.(a) The op amp in the bistable circuit of Fig.5(a) has output saturation of ±13 V. Design the circuit to obtain threshold voltages of ±5 V. For R_1=10 kΩ, find the value required for R_2.(3%)

(b) Provide a design of the inverting precision rectifier shown in Fig.5(b) in which the gain is -2 for negative inputs and zero otherwise, and the input resistance is 100 kΩ. What values of R_1 and R_2 do you choose?(3%)

(c) An op amp has a rated output voltage ±10 V and a slew rate of 1 V/μs. If an input sinusoid with frequency 5 times the full-power bandwidth is applied to an unity-gain follower constructed using this op amp, what is the maximum possible amplitude that can be accommodated at the output without incurring the slew-induced distortion ?(3%)

(d) A multiple amplifier having a first pole at 2 MHz and a dc open-loop gain of 80 dB is to be compensated for closed-loop gains as low as unity by the introduction of a new dominant pole. At what frequency must the new pole be placed?(3%)

(e) For the circuit shown in Fig.5(c), assume high β and BJTs having v_{BE}=0.7 V at 1 mA. Find the value of R that will result in I_o=10μA.(4%)

(f) The network shown in Fig.5(d) is used with an op amp to form an oscillator. What is the oscillation frequency and the minimum gain of the op amp. Draw the oscillator circuit.(6%)

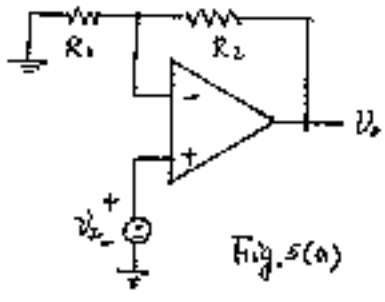

Fig. 5(a)

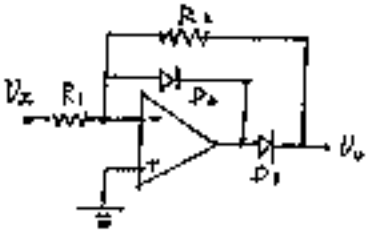

Fig. 5(b)

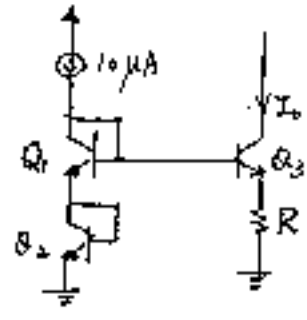

Fig. 5(c)

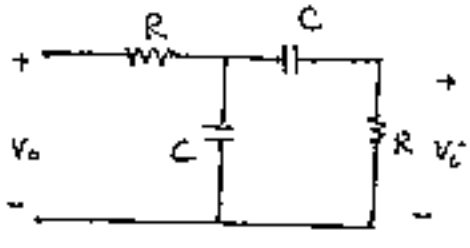

Fig. 5(d)