1: (15%) (本題全部以 16進位表示)
Given the diagram of Fig. 1, assume that the memory is designed to use the most space it can use.
(a) please determine the ranges of the I/O space and the memory space for the system.
(b) What is the address range used for the chip 8255? (以 16進位表示)
(c) For the I/O address scheme, is it a memory-mapped I/O or isolated I/O? Why?

2: (17%)
For a two-way set-associative cache memory with its content as shown in Fig. 2, given a memory read operation with the physical address of 1EE048,
(a)please determine whether a cache hit or cache miss will occur?
Explain the operation of the cache access to show the reason why.
(b)What value will be retrieved from this memory read? (以 16進位表示)
Note that the size of the cache is 16K bytes and the block size(cache line) is 16bytes. The fields in Fig. 2 represent the following meanings. V: 1 means this block is a valid block, 0 otherwise. D: 1 means a dirty block, 0 otherwise. F: 1 means the most recently used block, 0 otherwise.

3: (6%)
A system consisting of only one CPU, one disk controller, and main memory of 16M bytes, does not need bus arbitration scheme. Is this declaration true or false? Specify your reason.

4: (6%)
From a benchmark, we found that computer A which is a CISC computer runs faster than computer B which is a RISC computer. From this fact, it is concluded the computer A has higher MIPS than computer B. Is this declaration true or false? Specify your reason.

5: (6%)
Virtual memory is used to expand the physical address space. Is this declaration true or false? Specify your reason.

6. (17%) A sequential circuit has two D flip-flops A and B, two inputs x and y, and one output z. The flip-flop equations and the circuit output are as follows:

$$D_A = x'y + xA$$
$$D_B = x'B + xA$$
$$z = B$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.

7. (16%) Construct a diagram of a 8×8 omega switching network. Show the switch setting required to connect input 3 to output 1.

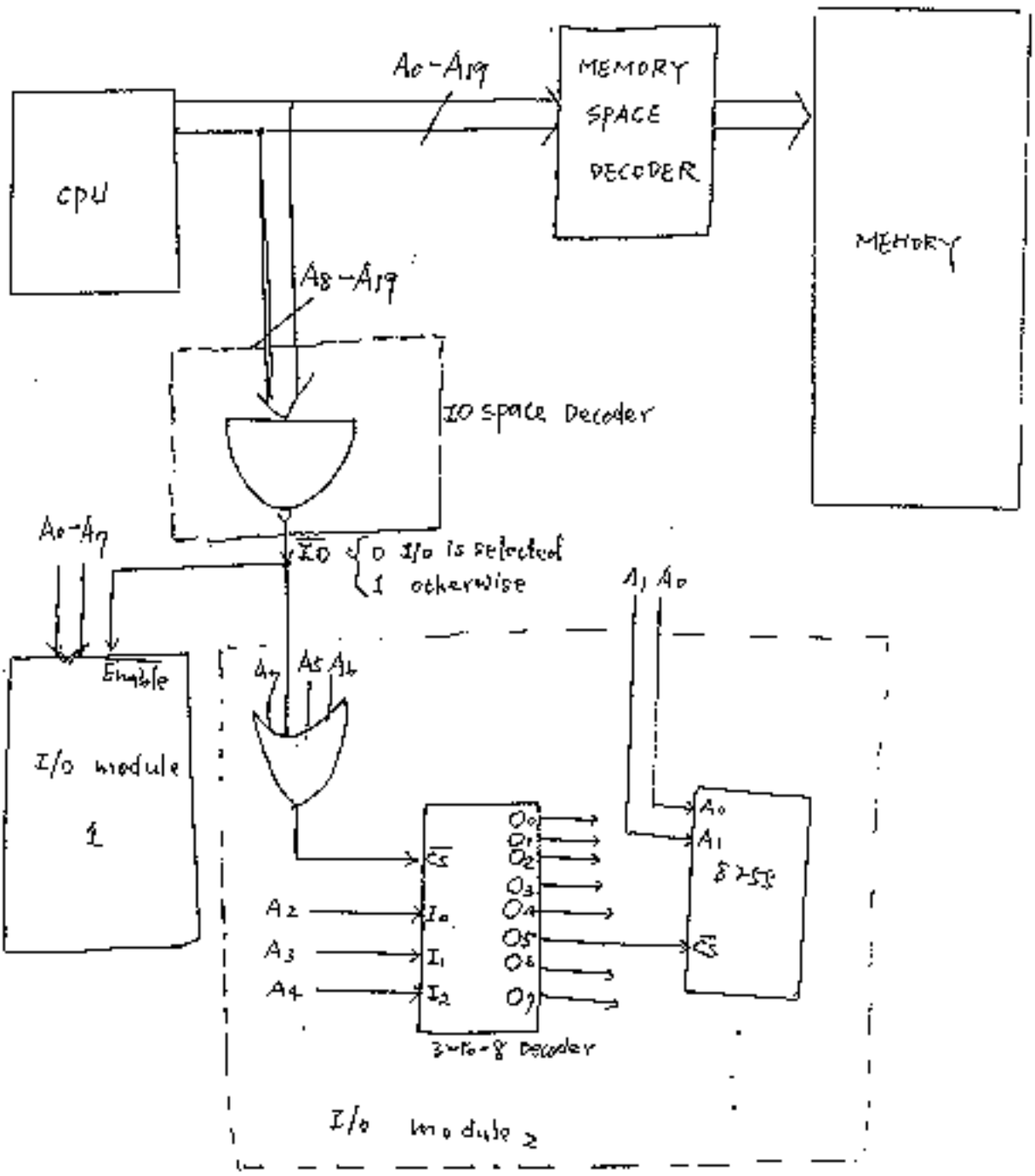
8. (17%) Consider the following two Boolean functions

$f = ADF + AEF + BDF + BEF + CDF + CEF + G$

$g = XYF + G$, where $X = A + B + C$ and $Y = D + E$

(1) Show that $f = g$.

(2) Which expression is better? Why?



Note: CS is the chip select, 0 means enable the chip to work, 1 otherwise

Fig1: A small computer system I/O space design

(背面仍有題目,請繼續作答)

	V	D	F	Tag	Data
0	1	0	0	7FF	35 67 EE FF 08 09 A0 78 56 74 35 11 22 00 99 67
1	1	0	1	238	8C 95 36 49 88 23 56 E0 47 98 AB CD EE FF 39 40
2	1	1	1	7FC	76 84 35 97 38 60 70 80 C8 9E F9 56 43 89 67 35
3	1	0	0	2EE	44 55 66 77 88 AA 11 22 37 45 56 23 E0 F7 93 15
4	1	0	1	0F7	25 66 89 CC DD C9 77 88 CD E9 86 03 45 23 98 77
5	1	0	0	388	36 C0 96 45 38 29 8E 07 67 E0 DD 96 54 39 26 78
.				.	.
.				.	.
.				.	.
1FF	1	1	1	42C	38 25 46 79 55 66 77 11 33 42 25 83 69 98 25 41

	V	D	F	Tag	Data
0	1	0	1	235	40 11 25 23 44 AA 0C 23 25 43 98 EE 78 45 26 00
1	1	1	0	278	A8 85 96 38 42 95 22 11 84 89 F0 4A 89 26 47 38
2	1	0	0	4A0	99 26 98 23 11 25 EE 86 33 2A 89 30 41 85 96 33
3	1	0	1	2FF	55 64 39 67 21 33 56 78 45 AA A0 E7 29 36 25 11
4	1	1	0	23C	12 35 24 33 11 25 67 88 19 11 25 44 38 78 11 33
5	1	0	1	45A	89 24 15 67 34 25 33 88 89 24 86 99 33 25 11 00
.				.	.
.				.	.
.				.	.
1FF	1	0	0	12A	EE F0 38 96 43 55 11 24 A0 78 25 43 21 47 35 26

Note that the data within each cache line (block) is placed by the following order:

byte	0	1	2	3	4	5	6	7
	8	9	A	B	C	D	E	F

Fig. 2: The cache content of the 2-way set-associative cache memory.