1. (a) A TTL NAND gate with a totem-pole output is shown in Fig.1A. Please estimate the (a) average static power dissipation $P_{(av)}$, and (b) dynamic power dissipation $P_{(dyn)}$ of this gate. (15%)

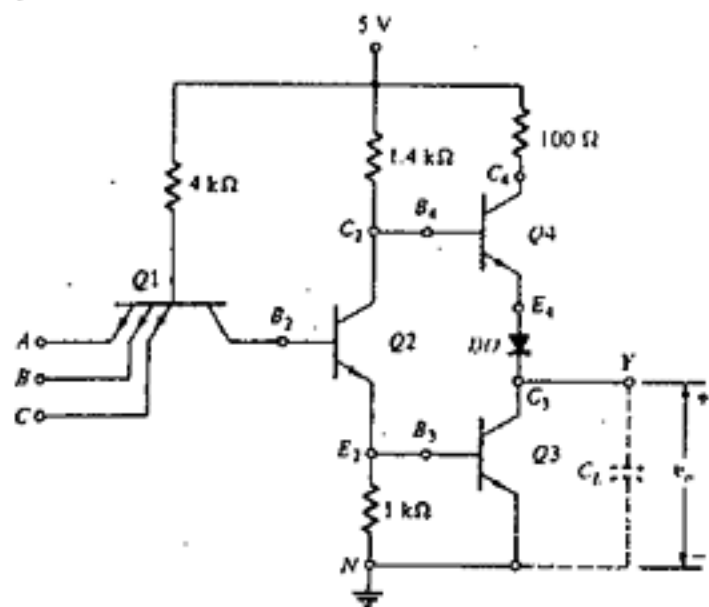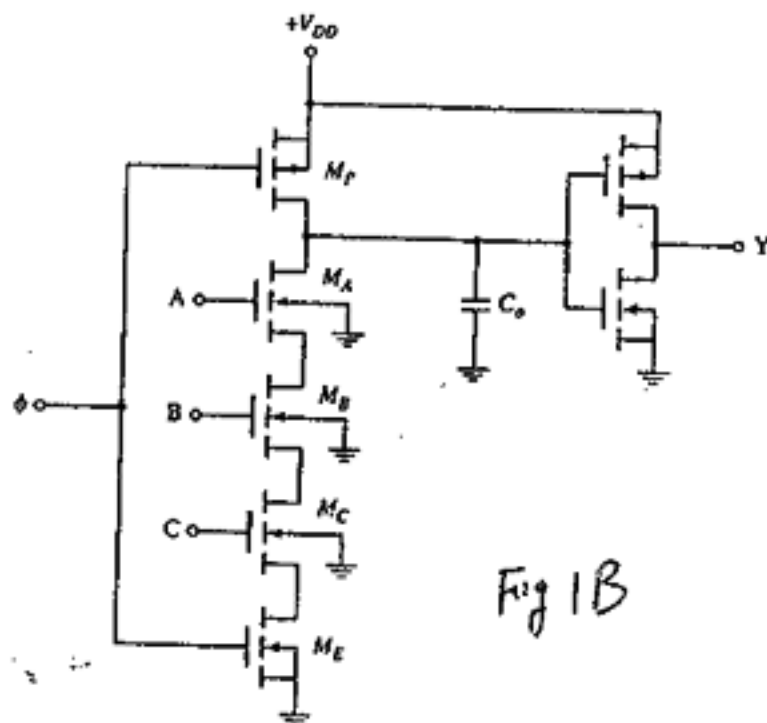(b) A domino logic circuit is shown in Fig.1B. What is the function realized at the output Y? (5%)

Fig 1A

Fig 1B

2. (A) 簡述(a)振盪器之振盪如何啓動？振盪器之優劣如何判斷？(4%)，(b)動態負電阻振盪器之操作原理(3%)？(c) Op-Amp 虛短路成立之條件(3%)。
(B) 求圖 2 所示放大電路之頻率增益乘積(GBP)值與截止頻率。設 $R_s = 0.25\ k\Omega$，$R_L = r_\pi = 1\ k\Omega$，$C_\pi = 100\ pF$，$C_\mu = 1\ pF$，$\beta = 100$。(10%)
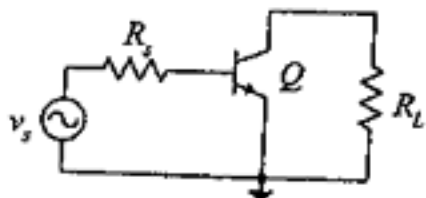

Fig 2

3. 簡述(a)頻率補償之意義及目的。(b)試利用波德圖說明如何判斷網路系統之穩定與不穩定。(10%)

4. (a) Calculate V_- and V_o of the circuit shown in Fig. 4(a) where the OPAMP gain = 10. (8%)
(b) Calculate V_+ and V_o of the circuit shown in Fig. 4(b) where the OPAMP gain = 10. (9%)
(c) Calculate V_+ and V_o of the circuit shown in Fig. 4(c) where the OPAMP gain = 1. (8%)
(V_-, V_+, and V_o are the inverting input voltage, noninverting input voltage, and output voltage of the OPAMP, respectively)
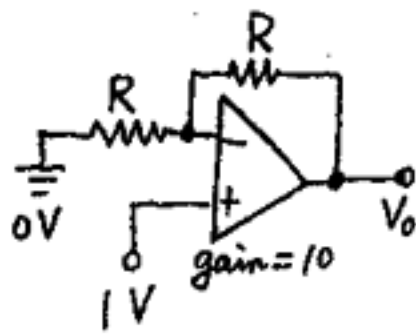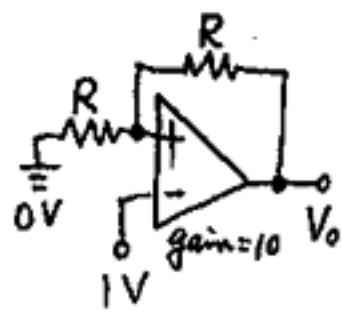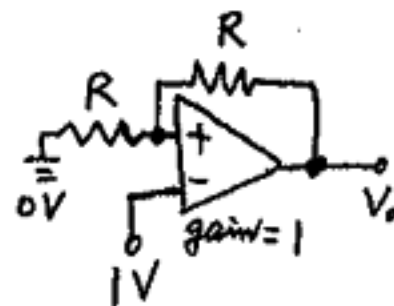
Fig. 4(a)   Fig. 4(b)   Fig.4(c)

5. For the circuit shown in Fig. 5, find the input resistance Ri and the voltage gain v_o/v_s. Assume that the source provides a small signal v_s and that β is high. Note that a transistor remains in the active region even if the collector voltage falls below that of the base by 0.4V or so. (10%)

6. For the common-base circuit shown in Fig. 6, assuming the bias current to be about 1mA, β=100, C_μ=0.8pF, and f_T=600MHz. Please (a) estimate the midband gain V_o/V_s. (b) use the short circuit time constants method to estimate the lower 3dB frequency f_L. (c) Find the high frequency poles, and estimate the upper 3dB frequency f_H. (15%)
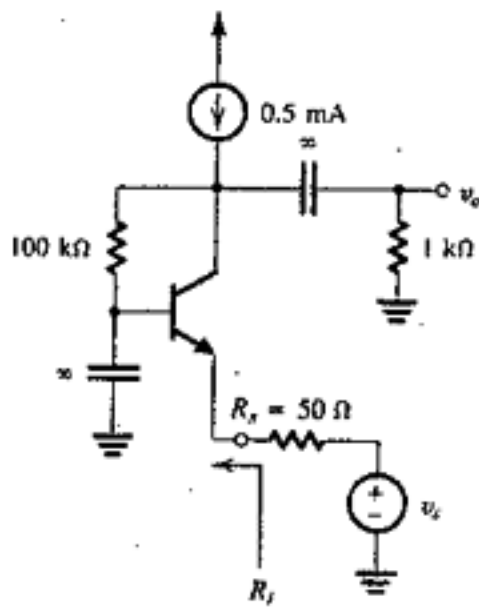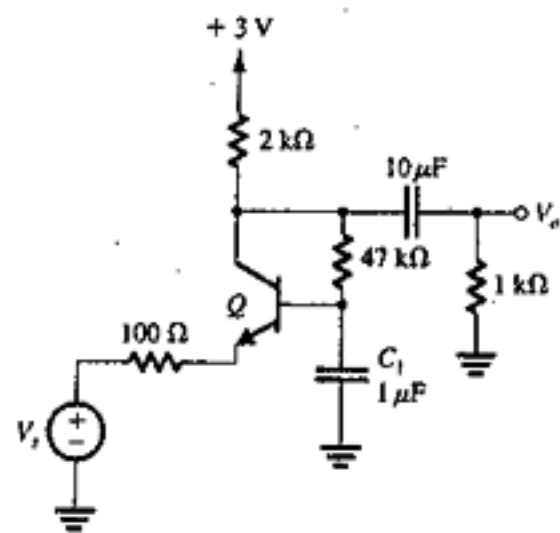

Fig 5.

Fig 6.

711>B