(10%)1: A computer system embedded with pipeline technique is destined to run faster than another of a same instruction set but without pipeline embedded. Is the statement correct? Specify your reason indicating when it is correct and when it is not.

(10%)2:VLIW is used in CPU design to improve its performance. However, the level of improvement heavily depends on the characteristics of the running program. If you were to write programs using its instruction set, what would you pay attention to, the most, on your programming so as to best gain the advantages of VLIW design?

(12%)3: Assume that you are given the instruction sets:

Move R, address
Store address, R
Input R, address
Output address, R

Where "Move R, address " is to move the content of memory at "address" into register R, "Store address, R" is to store the content of register R into memory location "address". The operation for "Input" and "Output " is similar to "Move " and "Store", except that they are designed for I/O operations. If you were to send the memory content at 0004 to an output port at FF04, please write instructions to accomplish this job when the system is designed using
(a) memory-mapped I/O
(b) isolated I/O.

(15%) 4: A virtual memory system has a page size of 1024 words, eight virtual pages, and four physical page frames. The page table is as follows:

virtual page number	page frame number
0	3
1	1
2	–
3	–
4	2
5	–
6	0
7	--

(背面仍有題目,請繼續作答)

(a) Make a list of all virtual addresses that will cause page faults.
(b) What are the main memory addresses for the following virtual address: 0, 3728, 1024, 1025, 4096.

(Note that the numbers in part (b) are all decimal numbers)

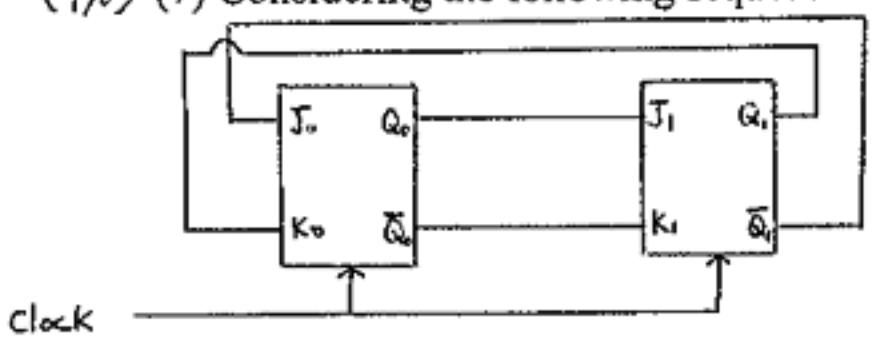
(10%) (4) The interrupt vector is used to indicate the interrupting sources and used to access the interrupt table so as to fetch the address of interrupt service routine from the interrupt table. Because of this reason, the interrupt vector is usually placed in the address line. Specify if the statement true or false and the reason why.

(24%) (5) Please briefly describe the following items:
(a) translation lookaside buffer
(b) data hazards
(c) load/store architecture
(d) interleaved memory

(10%)(6) Derive the duals of the following functions in sum-of-products form.
(i) $f = x_1\bar{x}_3(\bar{x}_2 + x_4) + x_4$

(ii) $f = \overline{\bar{x}_1 x_2 + \bar{x}_3 x_4}$

(9%) (7) Considering the following sequential circuit,



please use the given state encoding to complete the state diagram for the circuit.

Q_1	Q_0	state
0	0	0
0	1	1
1	0	2
1	1	3