1. Using the ideal op amp to implement two different non-inverting integrators without inverter. Explain your results in brief. (10%)

2. The op amp in the circuit of Fig. 1 has an open-loop gain of 10^5 and a single-pole rolloff with $\omega_{3dB} = 10$ rad/s.
   (a) Sketch a Bode plot for the loop gain. (2%)
   (b) Find the frequency at which $|A\beta| = 1$, and find the corresponding phase margin. (4%)
   (c) Find the closed-loop transfer function, including its zero and poles. (4%)

3. Why is Miller-effect compensation often employed to compensate an op amp? (10%)

4. Draw the circuit diagram of a 2-bit charge-redistribution A/D converter and explain its operational principle. (10%)

5. For the circuit shown in Fig. 2:
   (a) Calculate the emitter resistance of the T model (r_e), and base resistance of the hybrid-π model (r_π) of transistor Q_1. Use $\beta = 100$, $V_{BE(on)} = 0.7$V. (10%)
   (b) Calculate the input resistance (R_i) and the voltage gain (v_o/v_s). (10%)

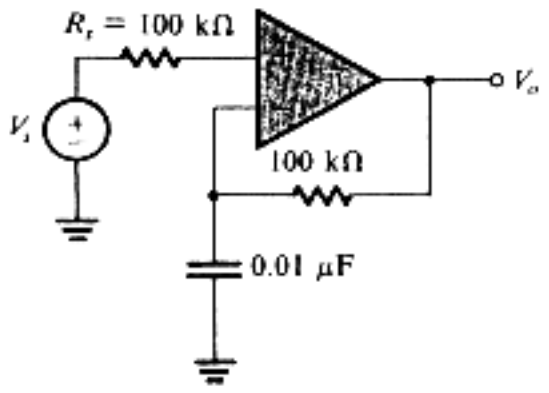

Fig. 1

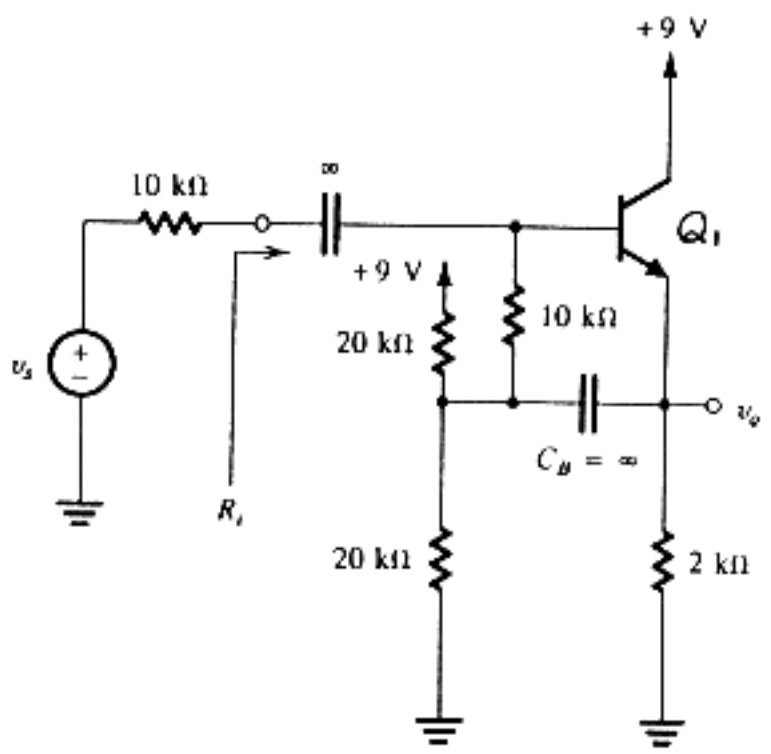

Fig. 2

6. For the circuit shown in Fig. 3, express I_o as a function of V_o. Assume that all transistors are identical with $V_{BE(on)} = 0.7V$ and $V_A = 120V$. (10%)

7. Calculate the bias current I_{bias} of the circuit shown in Fig. 4. Assume that threshold voltage of device M1 and M2 is identical, $\mu_n C_{ox} = 20\mu A/V^2$. (10%)

8. (a) Determine the logic function at the output Y of the circuit shown in Fig. 5A. (10%)
   (b) What is the logic function realized at Y in the NMOS circuit shown in Fig. 5B? (10%)

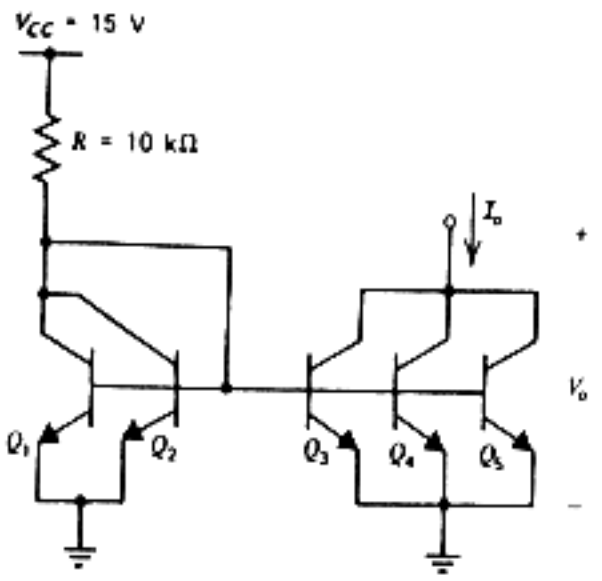

Fig. 3

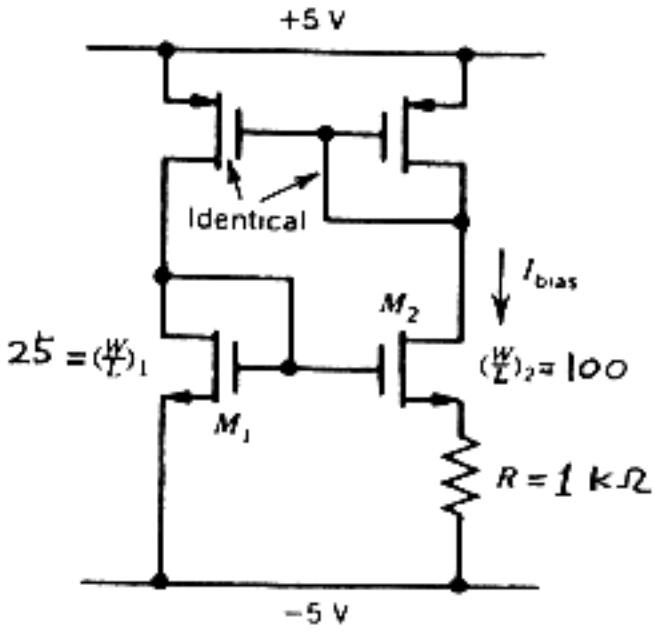

Fig. 4

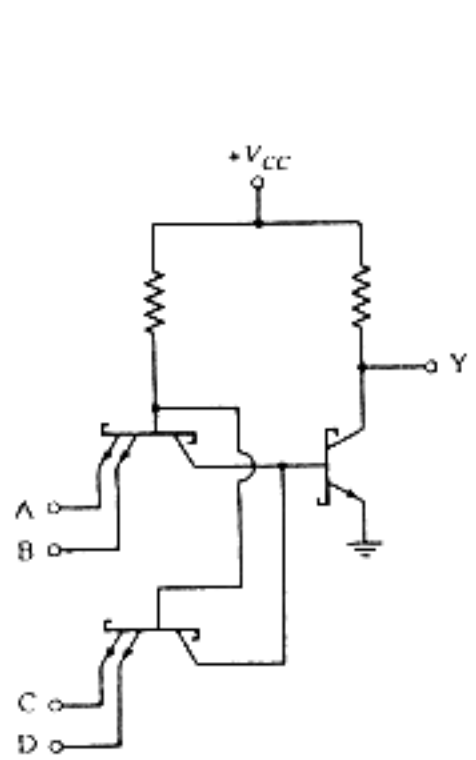

Fig. 5A

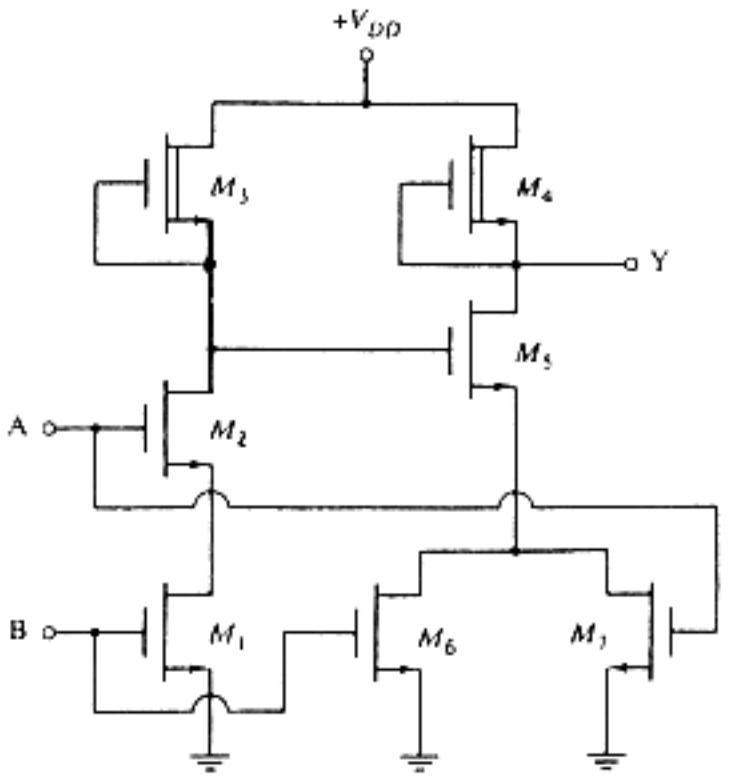

Fig. 5B