1. How many total bits are required to implement a direct-mapped cache with 64KB of data and one-word blocks assuming a 32-bit address? (1 word = 4 bytes) (10%)
2. Consider the following measurements made on a pair of SPARCstation 10s running Solaris 2.3, connected to two different types of networks, and using TCP/IP for communication. Find the host-to-host latency for a 250-byte message using each network. (20%)

Characteristic	Ethernet	ATM
Bandwidth from node to network	1.25 MB/sec	10 MB/sec
Interconnect latency	15 us	50 us
HW latency to/from network	6 us	6 us
SW overhead sending to network	200 us	207 us
SW overhead receiving from network	241 us	360 us

3. Our favorite program runs in 10 seconds on computer A, which has a 400MHz clock. We are trying to help a computer designer build a machine, B, that will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing machine B to require 1.2 times as many clock cycles as machine A for this program. What clock rate should we tell the designer to target? (20%)
4. Design the memory system for a microprocessor. Assume that the processor uses 32-bit logical address, 32-bit physical address, and 64-bit external data bus.
   a. Show the design of a 4-way set associative TLB. This TLB has 32 entries. The page size is 8KB. (10 %)
   b. Show the design of a two-way interleaving DRAM main memory system for this processor. The memory size is 256 MB using 8Mx4 DRAM chips. Assume that this memory is located at the lowest address space and the processor uses little endian mode. (10 %)
5. Explain the following terms (20 %).
   a. Write allocation
   b. Stack frame pointer
   c. Assembler directives
   d. Microprogram
6. a. Simplify F (a,b,c) = Σ m(0,1,2,5,6,7). (5%)
   b. Find the maxterm expansion of F. (5%)