1. Please write down the addressing modes of the MIPS instruction sets with brief explanation. (20%)

2. Suppose that 20% of the instructions are loads, and half of the time the instruction following a load instruction depends on the result of the load. If this hazard creates a single-cycle delay, how much faster is an ideal pipelined machine (with CPI of 2) that does not delay the pipeline, compared to this realistic pipeline that may create a single-cycle load stall delay? (Ignore any stalls other than load stalls) (20%)

3. Look at this code sequence
   SW 512(R0), R3; M[512] ← R3 (cache index 0)
   LW R1, 1024(R0); R1 ← M[1024] (cache index 0)
   LW R2, 512(R0); R2← M[512] (cache index 0)

   Assume a direct-mapped cache that maps 512 and 1024 to the same block, and a four-word write buffer. Will R3 always equal to R2? (10%)

4. Explain the following terms (20%)
   a. Microinstruction.
   b. Handshaking protocol.

5. In a multicycle implementation, (20%)
   a. Please specify each of the instruction execution steps of a load instruction (format: lw Ri, offset (Rj)).
   b. Assume that each step takes one CPU cycle to complete. Use a state diagram of five states to explain how a processor may handle an I/O interrupt that occurs during the execution of a load instruction?

6. The following figure shows the miss rate versus block size. Explain why these curves look like a smile curve, that is, higher miss rate at the two ends while lower miss rate in the middle. (10%)