1. a. The control unit of a processor can be implemented in a multi-cycle state machine. Does this control unit differ from a processor using single cycle implementation? What are the differences? Which one has a better performance? Why? (10%)

   b. Show the block diagram of a control unit implemented as a microcode controller (5%). How does this microcode controller execute a micro-program? (10 %)

2. a. What is a TLB? Is it necessary to flush the TLB when processor performs a context switching? Why ? 5%

   b. How to handle a TLB miss? 5%

3. A string of address references given as byte addresses is listed as follows: 1, 5, 8, 3, 40, 17, 19, 56, 49, 11, 14, 43, 20, 48, 79, 107. Consider a two-way set associative cache with a total of 8 lines and the line size is 4 bytes. Label each reference in the list as a hit or miss and show the final contents of the cache. Assuming that the lines are initially empty, LRU replacement policy is used, and Way 0 is allocated first. (10%)

4. a. Compare the differences between interrupt I/Os and polling I/Os. 10%

   b. What is an I/O port? What is a peripheral? Show a block diagram illustrating the relationship of an I/O port and a related peripheral. 10%.

   c. How to address a control register or a status register in an I/O port? 5%

5. If you are asked to design a RISC type processor, the processor will support only three types of addressing modes. What are the addressing modes you plan to design? Why? Show an example for each one you choose. 15%

6. a. Compare a direct jump and an indirect jump. 5%

   b. Write down three different types of instructions that can change the control flow of program executions. Why do we need them?   10%