

1. For the circuit shown in Fig.1, for the BJT,  $\beta=200$  and  $|V_A|=100V$ , and for the MOSFET,  $|V_A|=30V$ ,  $|V_t|=1V$ ,  $k'(W/L)=200\mu A/V^2$ . Let  $I=20\mu A$  and  $V_{BIAS}=2V$ . Assume the current generator  $I$  to have the same resistance as the output resistance of its connected circuit and assume the current generator  $2I$  to be ideal. Find
- the bias current in  $Q1$  (3%);
  - the voltage at the node between the two transistors (assume  $|V_{BE}|=0.7V$ ) (3%);
  - $g_m$  and  $r_o$  for each device (4%);
  - the maximum allowed value of  $v_o$  (3%);
  - the voltage gain (3%);
  - the input resistance (3%);
  - the output resistance (3%);
  - Does the current source  $2I$  have to be a sophisticated one? For this generator, what output resistance would reduce the overall gain by 1%? (3%)
2. Consider an OPAMP with  $V_{DD}=5V$ ,  $GND=0V$  and  $V_{SS}=-5V$  as shown in Fig.2.
- If  $R_1=R_2=1k\Omega$  and  $V_{in}=0V$ , please find that  $V_-=?$   $V_o=?$  when the OPAMP is with 10 mV input offset and gain  $A=\infty$ . (10%) ( $V_-$  is the inverting input node of the OPAMP)
  - If  $R_1=R_2=1k\Omega$  and  $V_{in}=2V$ , please find that  $V_-=?$   $V_o=?$  when the OPAMP is with 10 mV input offset and gain  $A=\infty$ . (5%)
  - If  $R_1=1k\Omega$  and  $R_2=1000k\Omega$ , please find that  $A_F=V_o/V_{in}=?$  when the OPAMP is with no offset and gain  $A=100$ . (10%)
3. A TTL NAND gate with a totem-pole output is shown in Fig.3. Assume that the inputs are derived from the outputs of identical gates and  $\beta_F=100$  and  $\beta_R=0.5$ .
- Given  $A=B=C=V(1)$ , determine the operation modes of transistors  $Q_1$  and  $Q_4$ . (4%)
  - Repeat (a) for the situation where at least one input logic level is  $V(0)$ . (4%)
  - Determine the logic levels. (8%)
  - Please estimate the average static power dissipation ( $P_{av}$ ) and dynamic power dissipation ( $P_{dyn}$ ) per gate. (9%)
4. (a) Draw the load line of  $D1$  and find  $V_I$  for the circuit shown in Fig. 4. Assume that  $D1$ ,  $D2$  and  $D3$  have the same I-V characteristics, and  $V_A=3V_r$ , where  $V_r$  is the cut-in voltage of the diode. (10%)
- (b) Derive and plot the small-signal equivalent circuit for a BJT with I-V characteristics expressed as  $i_C=av_{BE}^2(1+bv_{CE})$ , where  $a$  and  $b$  are constant. (5%)
- (c) Determine  $I_D$  and  $V_O$  for the circuit shown in Fig. 5 for  $V_{DD}=5V$  and  $V_I=2V$ . Assume that  $k_{n1}=5k_{n2}=50\mu A/V^2$  and  $V_{th1}=V_{th2}=1V$ , where  $k_n(=0.5\mu_n C_{ox}(W/L))$  is the conduction parameter and  $V_{th}$  is the threshold voltage. Note that  $T2$  is an enhancement-mode MOSFET. (10%)

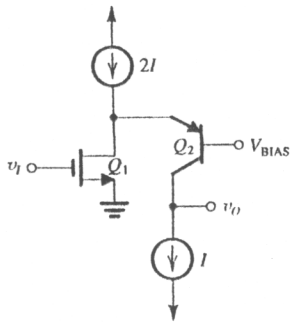


Fig. 1

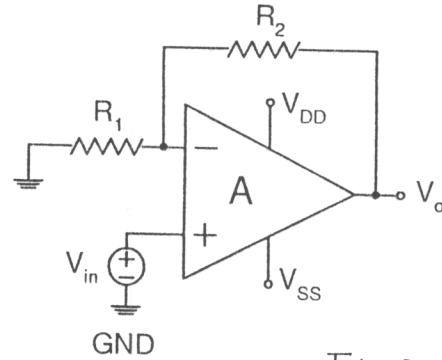


Fig. 2

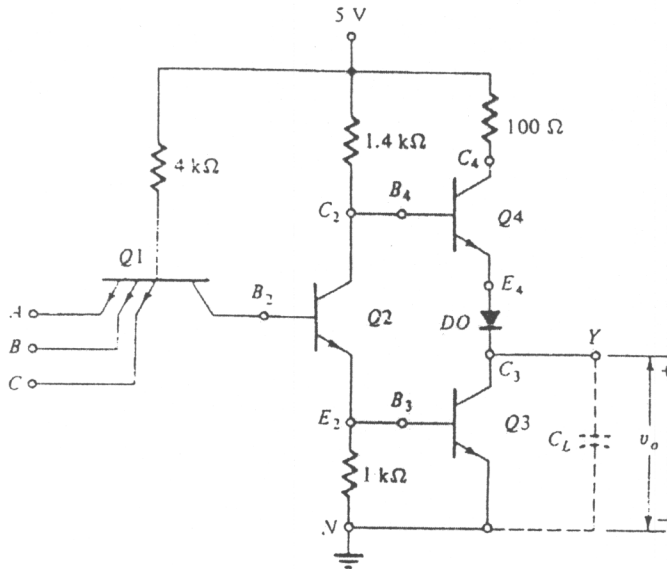


Fig. 3

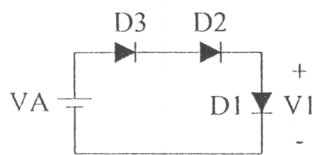


Fig. 4

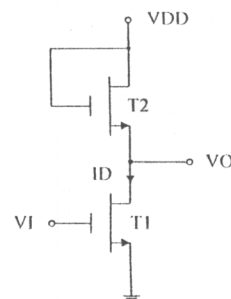


Fig. 5