1. For a five-stage pipeline that has IF, ID, EXE, MEM, and WB stage, describe how to design a forwarding unit to forward dependent source operands for a later instruction? State your assumptions for the instruction set and why the dependency may occur. (15%)

2. What is a branch hazard in a pipelined processor? What are the means to handle a branch hazard? Propose at least two means to solve a branch hazard. (20%)

3. Show the design of a direct-mapped write-back cache of 64KB. The line size is 32 bytes in length. It uses physical address for tags. Assuming the cacheable memory area is 256MB. Show the block diagram of the design, including tag memory, data memory, and buses. What is the replacement policy used in this design? (15%)

4. Design a DMA controller. Show a detailed block diagram of a DMA controller, including registers used. Describe the operation of a DMA controller. (20%)

5. Design an I/O port. What registers are required in a general I/O port? Why? (10%)

6. Explain the following terms for cache memories: (20%)
   a. Write-invalidate
   b. Cache coherency
   c. Write-allocate
   d. Temporal locality