1. Explain the design of the control unit of a microprocessor using multicycle implementation. Show a block diagram to explain such a design in general. Does this control unit differ from the control unit of the same processor using single cycle implementation? What are the differences? (20 %)
2. Answer the following questions about virtual memory. (35 %)
   a. What is a page fault? What event triggers a page fault? 5%
   b. Elaborate the procedure of handling a page fault. You may state your assumptions. 10%
   c. What is a TLB miss? What event triggers a TLB miss? 5%
   d. Elaborate the procedure of handling a TLB miss. You may state your assumptions. 10%
   e. Does a task have its own page table or all the active tasks share a page table? Why? 5%
3. In a pipelined processor, multiple interrupts may occur at the same clock cycle. Assume that an illegal instruction is detected at the ID stage and a load access exception occurs at the MEM stage at the same clock. Also assume that the processor has a five-stage pipeline and instructions are executed in-order. Answer the following questions: (30%)
   a. What are the causes that may result in an illegal instruction? 7 %
   b. What are the causes that may invoke a load access exception? 8 %
   c. Elaborate the procedures that handle these two interrupts occurring at the same clock. State the detailed operations of the pipeline control for these two events, one by one. 15 %
4. In a five-stage pipeline processor, the processor accesses the cache memories in the IF and MEM stage (if necessary). This may cause an instruction fetch miss or a data cache miss. Suppose that a cache-hit cycle takes one CPU clock. In this case, the processor does not have to stall the pipeline for cache hits. However, cache misses do occur and may take multiple CPU clocks to complete. Answer the following questions: (15%)
   a. If only the IF cache miss occurs, how does the processor pipeline handle this event? 4 %
   b. Repeat (a) when only the MEM cache miss occurs. 3 %
   c. What if the IF cache miss and the MEM cache miss occur at the same clock cycle? Elaborate the pipeline control procedures for these two misses that occur at the same clock cycle. 8 %