本試題是否可以使用計算機：☑可使用　，　☐不可使用　（請命題老師勾選）

1. **(15%)** A typical hypothetical microprocessor **pipeline** with 5-stage is shown in Fig. 1. Explain the function of the 5-stage (IF, ID, ALU, MEM, WB) instruction pipeline.

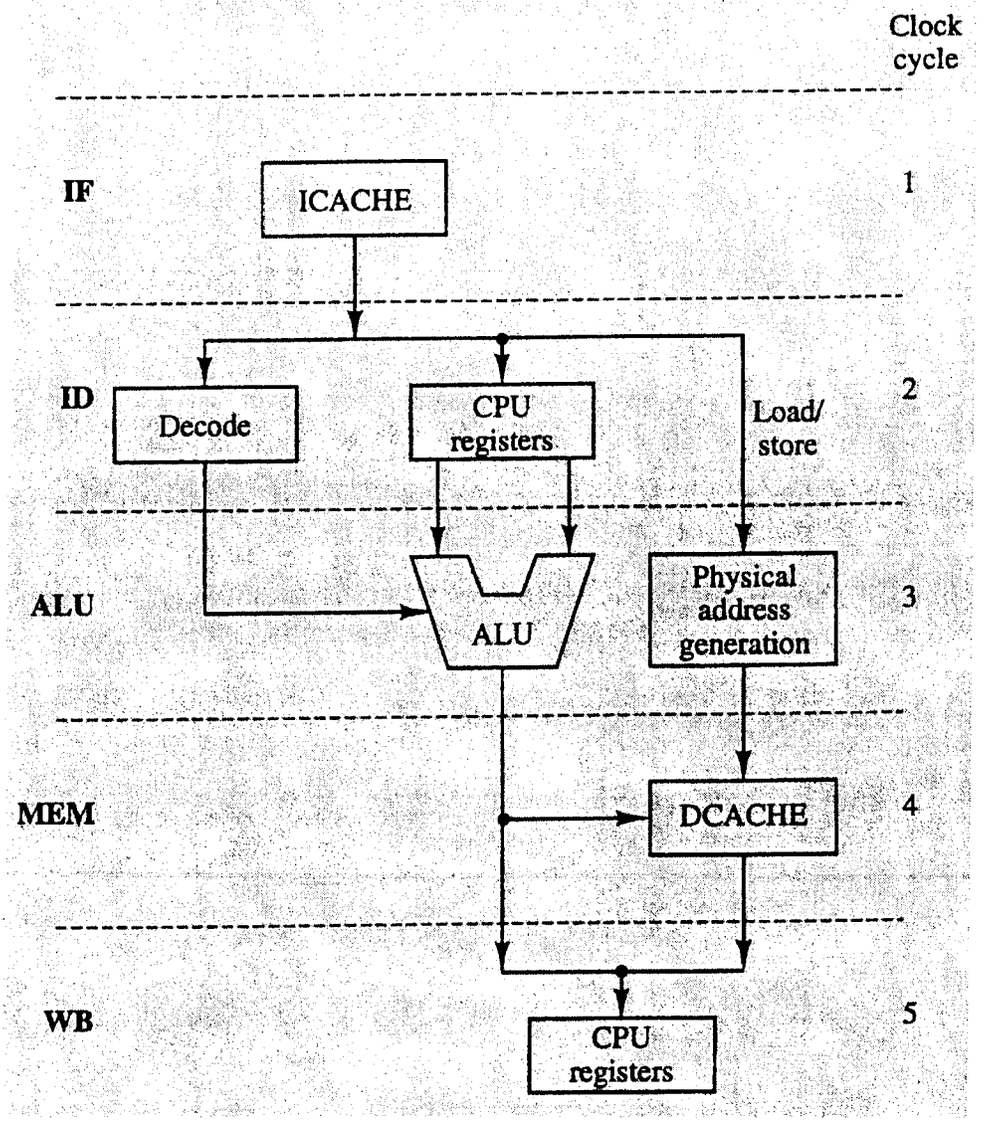

Fig. 1

2. **(15%)** The bandwidth of memory is usually smaller than that of the microprocessor, what techniques can be used to **increase the memory bandwidth**?
3. **(20%)** Describe and explain types of 68000 exceptions: (a) **external hardware exceptions** (*user interrupts, reset, bus error* signal), (b) **internal exceptions** (*address error, illegal instruction, unimplemented instruction, privilege violation, trace exception*, and *divine by zero*), and (c) **software exceptions** (by executing instructions *TRAP*, *TRAPV*, and *CHK*).

（背面仍有題目，請繼續作答）

4. **(15%)** Describe how **pipeline**, **superpipeline**, and **superscalar** decrease CPI (clock cycles per instruction) to increase the microprocessor performance.

5. **(15%)** For memory management, describe **paging** and **segmentation** skills and compare their differences.

6. **(20%)** Regarding to system bus, explain **mad-endian** (or Type-2) bus and **sad-endian** (or Type-1) bus. How are both buses related to **big-endian** and **little-endian** processors?