系所組別： 電機工程學系丁、戊組

考試科目： 計算機組織

※ 考生請注意：本試題 □可 ☑不可 使用計算機

1. Please describe the four steps in transforming a C program in a file on disk into a program running on a computer and show the translation hierarchy. (10%)

2. The following C program is run (with no optimizations) on a processor with a cache that has eight-word (32-byte) blocks and holds 256 bytes of data:

```
int i, j, c, stride, array[512];
....
for (i=0; i<10000; i++)
    for (j=0; j<512; j=j+stride)
        c = array[j]+17;
```

If we consider only the cache activity generated by references to the array and we assume that integers are words, what is the expected miss rate when the cache is direct mapped and stride=256? How about if stride =255? Would either of these change if the cache were two-way set associative? (20%)

3. (a) A compiler designer is trying to decide between two code sequences for a particular computer. The hardware designers have supplied the following facts:

	CPI for this instruction class		
	A	B	C
CPI	1	2	3

For a particular high-level-language statement, the compiler writer is considering two code sequences that require the following instruction counts:

	Instruction counts for instruction class		
Code sequence	A	B	C
1	2	1	2
2	4	1	1

Which code sequence executes the most instructions? Which will be faster? What is the CPI for each sequence? (10%)

(b) Consider the computer with three instruction classes and CPI measurements from (a). Now suppose we measure the code for the same program from two different compilers and obtain the following data:

	Instruction counts (in billions) for each instruction class		
Code from	A	B	C
Compiler 1	5	1	1
Compiler 2	10	1	1

Assume that the computer's clock rate is 4 GHz. Which code sequence will execute faster according to MIPS? According to execution time? (10%)

(背面仍有題目,請繼續作答)

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4. Assuming that we have a 5-stage pipeline processor implementing MIPS like ISA and branches are predicted to be not-taken for the pipeline operation. Answer the following questions for the following instruction sequences:

```
I1:   add r3, r5, r6   // first instruction to enter pipeline
I2:   beq r2, r4, labelx
I3:   sub r1, r1, r4
....
```

   a. Show the instruction format of the beq r2, r4, labelx instruction. Explain the usage of each field.(5%)
   b. What software tools are used to compute the value of labelx.(10%)
   c. Show the pipeline design that handles the control hazard should a misprediction occur. State your assumptions.(10 %)
   d. How many instructions are flushed by your design for control hazard handling?(5%)

5. Fill in the best appropriate answer for each of the following questions. (Only accept answers in English.)
   a. The space on the disk reserved for the full virtual memory space of a process is called _____.(5%)
   b. A _____ is the table which contains the virtual to physical address translation in virtual memory system.(5%)
   c. A _____ is a common variation of assembly language instruction that is used to simplify translation and programming but the hardware need not implement these instructions.(5%)
   d. A sequence of instructions without branches (except at possibly at the end) and with branch targets or branch labels (except possibly at the beginning) is called a _____.(5%)