※ 考生請注意：本試題 ☑可 ☐不可 使用計算機

1. A full-wave rectifier circuit shown in Fig. 1 is to deliver 0.1 A and 15 V (average) to a load R. The ripple voltage is to be no larger than 0.4 V peak-to-peak. The input signal V_I is 120 V (rms) at 60 Hz. Assume diode turn-on voltages of 0.7 V. Determine the required turns ratio (N_1/N_2) and the filter capacitance C value. (11%)

2. A CMOS inverter circuit shown in Fig. 2 has the parameters of V_{DD}=5 V, V_{TN}=-V_{TP}=1 V, K_N=100 μA/V^2, and K_P=50 μA/V^2. Determine the values of noise margins (NM_L, NM_H) and the gate threshold voltage V_M. (22%)

3. (a) Explain briefly why BJTs and FETs can amplify ac signals? (6%)
   (b) Redefine the small-signal parameters of the transistor to absorb the emitter resistance R_E in Fig. 3 (*i.e.*, to find g_{m2}, $r_{\pi 2}$, and r_{o2} in terms of g_{m1}, $r_{\pi 1}$, and r_{o1}). (6%)
   (c) A single BJT amplifier is needed that has a gain of ~0 dB and an input resistance of 25 MΩ with a load resistance of 25 kΩ. What is the preferred choice of amplifier configuration? Explain why you made this selection. (4%)

4. (a) Derive i_{out} and R_{out} for the circuit shown in Fig. 4. Assume the small-signal parameters of the MOSFET are g_m and r_o. (8%)
   (b) The MOSFETs in the circuit of Fig. 5 are matched, having $k_n'(W/L)_1 = k_p'(W/L)_2 = 1.5\ \text{mA/V}^2$ and $|V_t| = 0.5$ V. For G and D open, find the drain currents I_{D1} and I_{D2}. For $r_o = \infty$, what is the voltage gain of the amplifier from G to D? (10%)

(背面仍有題目,請繼續作答)

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5. Consider the circuit as shown in Fig. 6. The circuit is biased with V_{cc} = 12 V, and the load resistance is R_L = 75 Ω.

   The device parameters are :

   $I_{SD} = 5\times10^{-13}$ A for D_1 and D_2,

   $I_{SQ} = 2\times10^{-13}$ A , $\beta_n = \beta_p = 60$ for Q_n and Q_p.

   (a) Neglecting base currents, determine the required value of I_{Bias} such that the quiescent currents in Q_n and Q_p are I_{CQ} = 5 mA. (6%)

   (b) Find i_{cn} , i_{cp} , V_{BEn} , V_{EBp} , and I_D when V_o=2 V. (8 %)

   (c) What is the power conversion efficiency for this circuit when the output is a sinusoid and the peak output voltage reaches 80 percent of V_{cc}? (8%)

6. Consider the phase-shift oscillator shown in Fig. 7, with parameters C = 100 pF and R = 10 KΩ.

   (a) Determine the frequency of oscillation. (6%)

   (b) Find the minimum required value of R_2 for sustaining oscillation. (5%)

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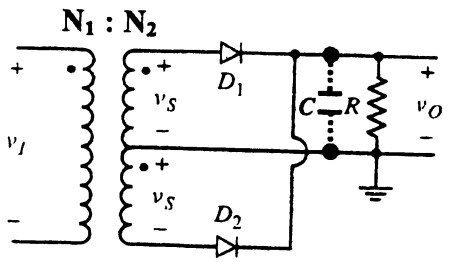

Fig. 1

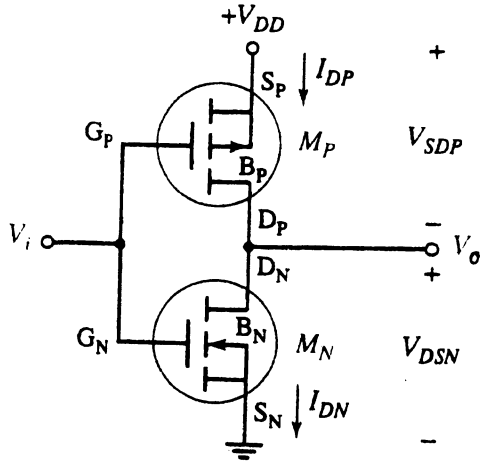

Fig. 2

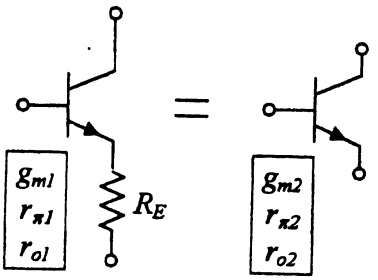

Fig. 3

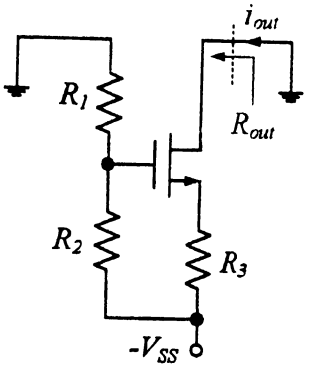

Fig. 4

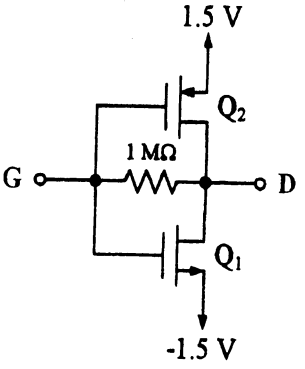

Fig. 5

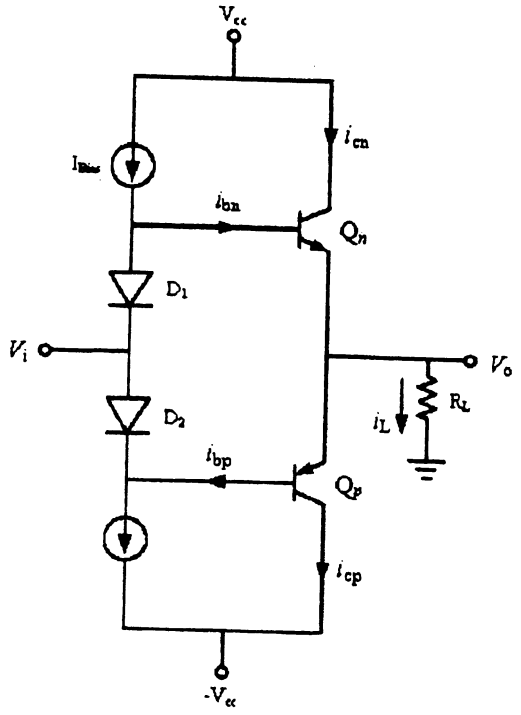

Fig. 6

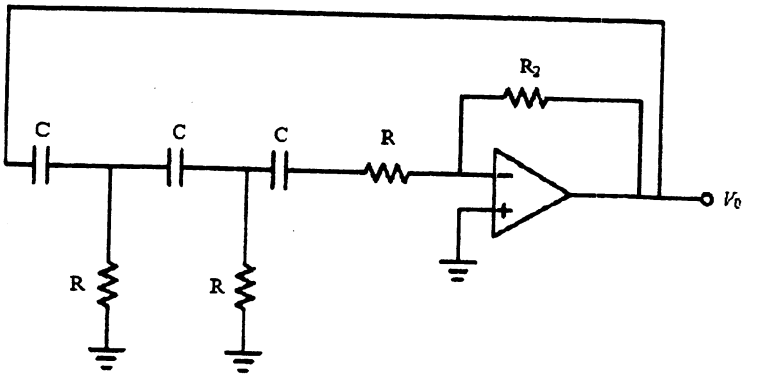

Fig. 7