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1. Design an address-translation cache or TLB for the following virtual memory system: virtual address =32 bits, physical address = 32 bits. The design should show how the virtual address is used and how a physical address is generated.
   a. Show a four-way set associative design assuming page size equal to 8KB. 10%
   b. Show a fully-set associative design assuming page size equal to 256KB. 10%
   c. Elaborate the procedure of handling a TLB miss. State your assumption. 10%

2、True or false 2% each.
   a. It is possible that a memory access results in a TLB miss, a page table hit, and a cache miss.
   b. It is impossible that a memory access results in a TLB hit, a page table hit, and a cache miss.
   c. It is possible that a memory access results in a TLB miss, a page table hit, and a cache hit.
   d. An I/O device raises a signal to inform the processor that it requires attention of the processor. This process is called polling and often used with a fast I/O.
   e. A write-back cache allows the CPU to write data into the cache without updating the main memory or the next level of memory. On the other hand, for a write-through cache, the written data are also updated in the main memory or the next level of memory.
   f. A 64K × 8 SRAM chip has 19 bits of the address bus.
   g. Pipelining instruction cache access improves the instruction throughput rather than individual instruction fetch latency.
   h. Pipelining instruction cache access improves the instruction throughput other than individual instruction fetch latency.
   i. Writing data into a flash memory is faster than reading the data out of the flash memory.
   j. NAND flash is much less expensive per gigabyte but memory could only be read and written in blocks.

(背面仍有題目,請繼續作答)

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3. A compiler designer is trying to decide between two code sequences for a particular computer. The hardware designers have supplied the following facts:

	CPI for this instruction class		
	A	B	C
CPI	1	2	3

For a particular high-level-language statement, the compiler writer is considering two code sequences that require the following instruction counts:

	Instruction counts for this instruction class		
Code sequences	A	B	C
1	2	1	2
2	4	1	1

a. Which code sequence executes the most instructions? 6%
b. Which will be faster? 6%
c. What is the CPI for each sequence? 6%

Suppose we measure the code for the same program from two different compilers and obtain the following data:

	Instruction counts(in billions) for each instruction class		
Code from	A	B	C
Compiler 1	5	1	1
Compiler 2	10	1	1

Assume that the computer's clock rate is 4 GHz.

d. Which code sequence will execute faster according to MIPS? 6%
e. According to execution time? 6%

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4. Do we need combinational logic, sequential logic, or a combination of the two to implement each of the following: 20%

a. multiplexor 2%

b. comparator 2%

c. incrementer/decrementer 2%

d. barrel shifter 2%

e. multiplier with shifters and adders 2%

f. register 2%

g. memory 2%

h. ALU (the ones in single-cycle and multiple-cycle datapaths) 2%

i. carry look-ahead adder 2%

j. latch 2%