

一. (1) 对图 1 之 Switched Capacitor 电路而言, 试绘出 ϕ 与 $\bar{\phi}$ 之控制讯号波形
 (b) 其所代表的一般电路之电路图。

(2) 试绘出图 2 电路的等效 Switched Capacitor 电路。

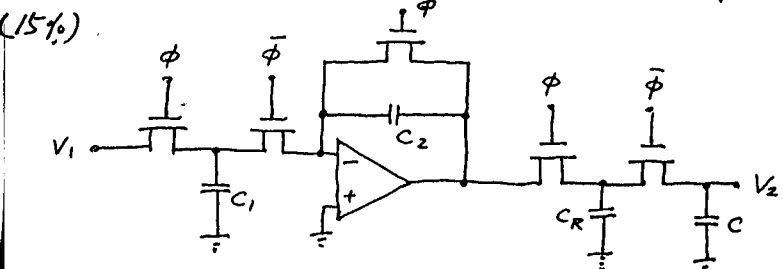


图 1.

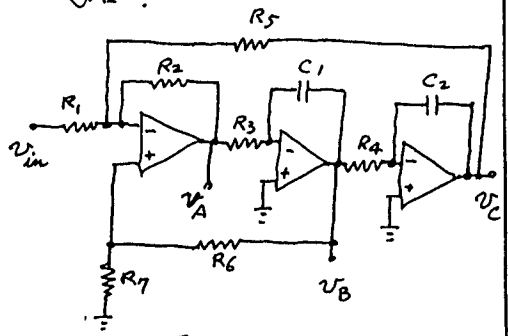
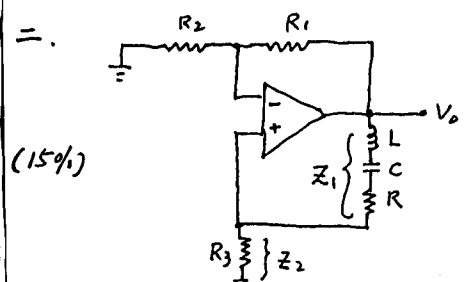


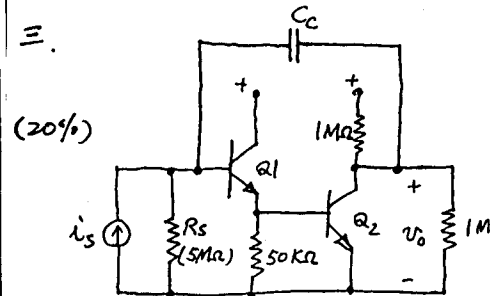
图 2.



(15%)

对左图之 Wien-Bridge Oscillator 而言, 试

- (1) 导出振荡频率
- (2) 求出 R_1/R_2 之最小比值。

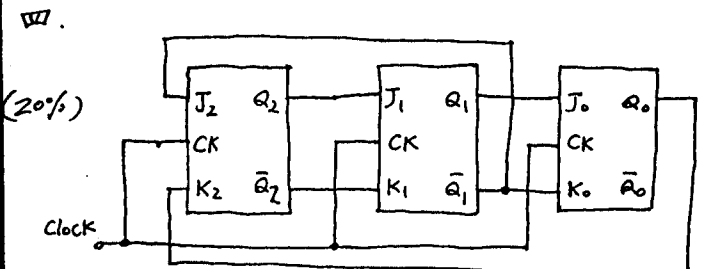


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左图中之电晶体 Q_1 与 Q_2 特性相同, 其 $\beta_0 = 250, V_A = 125V$

$f_T = 400MHz, C_{\mu} = 0.5PF; I_{C_{Q1}} = 5\mu A, I_{C_{Q2}} = 250\mu A.$

- (1) 於 $\omega = 0$ 时, 试求 R_i, R_o 与 V_o/I_s
 - (2) 若 Dominant Pole frequency 为 $10Hz$, 试求 C_c .
- [註] $\beta_0 = ac$ CE forward short-circuit current gain.
 C_{μ} = depletion region capacitance of the reverse-biased CB junction.
 V_A = Early Voltage.
- f_T = the frequency at which the CE short circuit current gain has unit magnitude.



(20%)

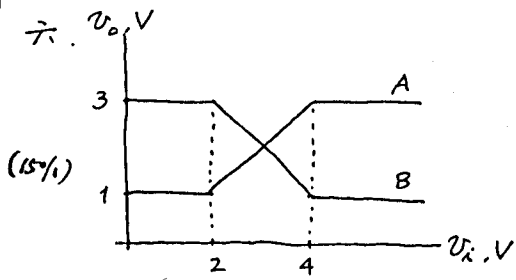
- (1) 左图电路中, 若起始状态为 $Q_0=0, Q_1=0, Q_2=1$, 试列出每一 Clock pulse 输入之后 Q_0, Q_1, Q_2, J_2, K_2 之状态变化表且问经过多少 Clock pulse 之后才会完成一个循环? (亦即左图为除以多少的 Counter)

(2) 若起始状态为 $Q_0=0, Q_1=1, Q_2=0$, 请重复 (1) 之问题。

五. Use a multiplexer to generate the combinational-logic equation

$$Y = \overline{DCBA} + DC\overline{BA} + D\overline{C}B\overline{A} + \overline{D}C\overline{B}A + DC\overline{B}A + \overline{D}C\overline{B}A + DC\overline{B}A + \overline{D}C\overline{B}A$$

(15%) How many data inputs are needed? Find the values of the data inputs X.



(a) A sinusoid $v_i(t) = 3 + 2 \sin \omega t$ is applied to a diode network whose voltage transfer characteristic is denoted by A. Sketch the output waveform $v_o(t)$ for one cycle.

(b) What changes would you expect in the output waveform if B is the voltage transfer characteristic of the network?

(c) Using ideal diodes, design a circuit having the A characteristic.