1. (15 %) Describe the following terminologies:
   (a) programmable logic arrays (PLA); (b) fan-in/fan-out;
   (c) Schottky TTL; (d) emitter-coupled logic (ECL);
   (e) field-programmable gate arrays (FPGAs).

2. (15 %) Fig. 1 depicts the circuit of a Schmitt trigger. Let the output
   levels be ± 5 V, i.e. $V_o = + 5$ V or - 5 V. Assume that the hysteresis
   voltage (V_H, the difference between high level threshold (V_1) and low
   level threshold (V_2)) is 0.1 V.
   (a) By giving $V_A = 1$ V, please derive $R_2/(R_1 + R_2)$ as well as V_1 and
   V_2.
   (b) Please give an arbitrary waveform input (V_{in}) and plot the resulting
   response of the inverting Schmitt trigger, V_o. Label appropriately the
   threshold voltages, V_1 and V_2.

Fig. 1

3. (20 %) In Wien bridge oscillator of Fig. 2, $R = 3$ $K\Omega$, $C= 500$ pF, and
   $R_d = 2$ $K\Omega$.
   (a) Determine the loop gain.
   (b) Find the resonant frequency.
   (c) Design a RC phase-shift oscillator at the same frequency of the Wien
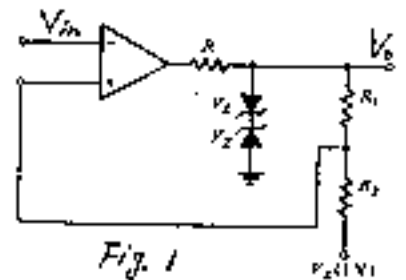   bridge oscillator.
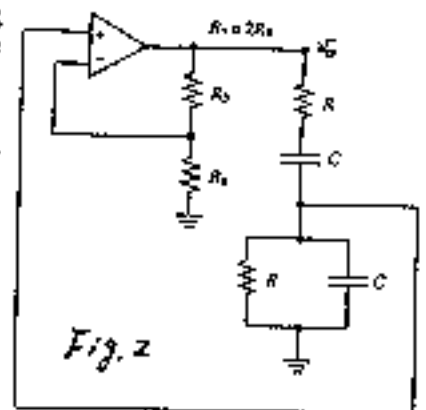

Fig. 2

4. (15%) For the circuit in Fig. 3, $R_0 = 1$ $K\Omega$, $R_1 = 2$ $K\Omega$, $R_2 = 4.7$ $K\Omega$,
   and $C= 10$ pF.
   (a) Determine $G(j\omega) = |Vo(j\omega)/Vi(j\omega)|$.
   (b) Plot $G(j\omega)$ versus frequency using bode approximations.
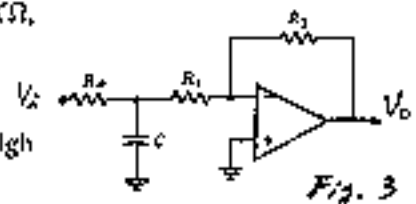   (c) Draw the equivalent circuit for $G(j\omega)$ at very low and at very high
   frequency.

Fig. 3

5. (15 %) Assuming that the op-amps in Fig. 4 are ideal, find the V_o/V_i
   and frequency response of input impedance, $Z_{in}(j\omega)$. (Let $R_1 = 1$ $K\Omega$,
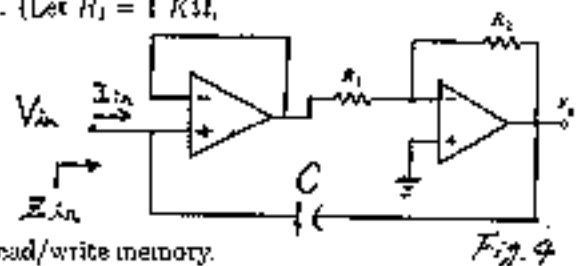 $R_2 = 15$ $K\Omega$, and $C= 100$ pF.)

Fig. 4

6. (20 %) Fig. 5 is a simple SR flip-flop served as 1-bit read/write memory.
   Please describe how to read data out or to write data into to the cell.
   (Hint: please give the logic states for X address, write enable, S, R, Q,
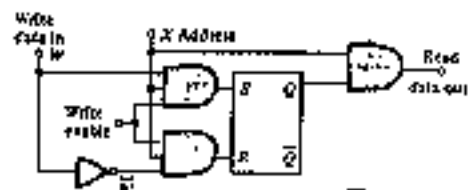   and data read out.)

Fig. 5