編號： 187、205

國立成功大學 105 學年度碩士班招生考試試題

系　　所：電機工程學系、電機資訊學院-微電、奈米聯招

考試科目：電子學

考試日期：0227，節次：1

※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. An ideal 9V Zener diode with zero incremental resistance is used in Fig. 1 for achieving voltage regulation.
   (a) What is maximum load current I_L that can be drawn from the regulator if it is to maintain a regulated output? (5%)
   (b) What is the minimum value of R_L that can be used and still have a regulated output voltage? (5%)

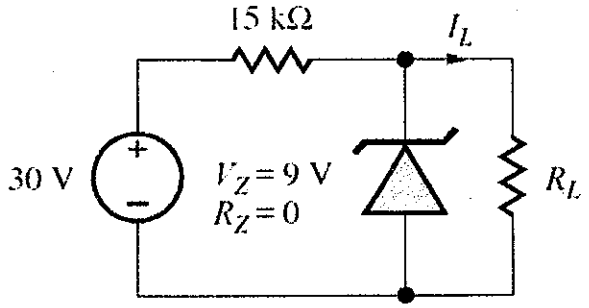

Fig. 1

2. Consider the amplifier circuit shown in Fig. 2, assume the transistor has β=100, V_{BEQ}=0.7V, and V_A (Early voltage) =100 V.
   (a) Find the dc bias current I_{CQ}. (4%)
   (b) Calculate the overall (mid-band) voltage gain v_o/v_{sig}, assume that C_1-C_3 are all shorted (8%)
   (c) What are the functions of capacitors C_1, C_2, and C_3? (3%)

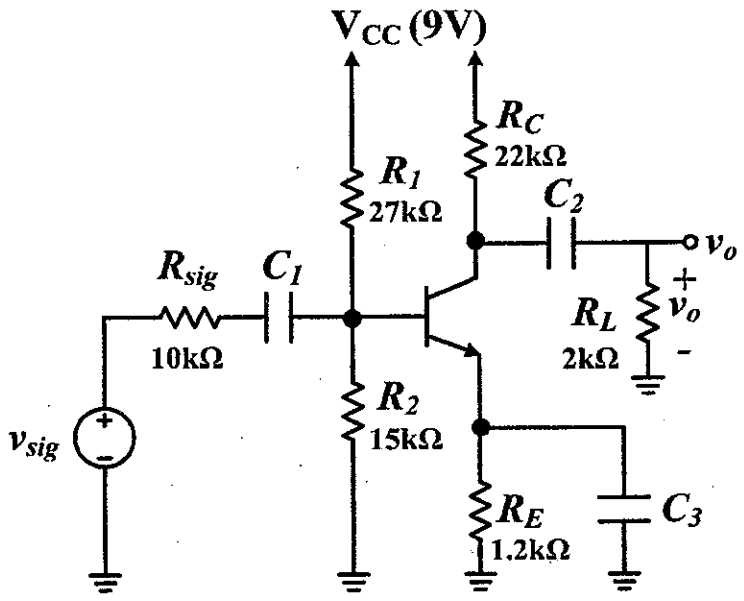

Fig. 2

3. Consider the single amplifier biquad filter shown in Fig. 3, assume ideal operational amplifier is used.
   (a) Please derive the transfer function, $V_O(s)/V_i(s)$, and find out its ω_0 and Q. (6%)
   (b) To realize a low-pass filter with f_0=4 KHz and maximally flat response, find the required values for C_1 and C_2, if R_1=R_2=10 KΩ. (4%)

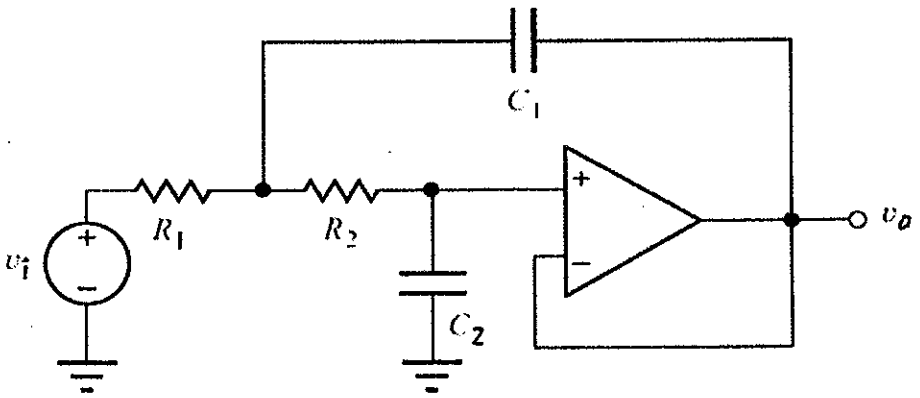

Fig. 3

4. Consider the circuit shown in Fig. 4, assume ideal operational amplifier is used.
   (a) Please analysis and draw v_o-v_i transfer curve. (5%)
   (b) For a triangular input waveform, please draw the corresponding output voltage waveform (correct scale required). (5%)

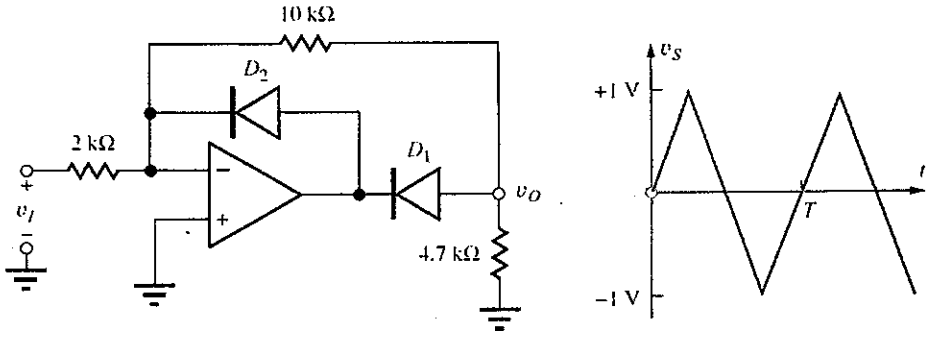

Fig. 4

5. The maximum junction temperature rating of a certain power transistor is 200°C. For a case temperature of 25°C, the maximum allowed power dissipation is 15W.
   (a) Find the junction-to-case thermal resistance. (2%)
   (b) If this transistor is operated with a case-to-sink thermal resistance of 1°C/W in an ambient temperature of 75°C and with a power dissipation of 5W, find the maximum allowed sink-to-ambient thermal resistance. (3%)

6. As shown in Fig. 5, the op amp is ideal.
   (a) Find the resistance looking into node 4, R_4, in terms of R.(4%)
   (b) Find the current I_4 in terms of the input current I. (4%)
   (c) Find the voltage at node 4, that is V_4, in terms of (IR) (4%)

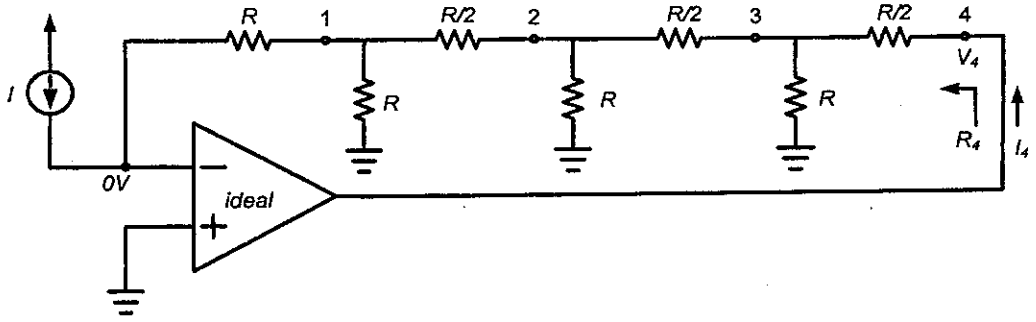

Fig. 5

7. Considering the design error because of the gross mismatch in the circuit of Fig.6. Specifically, Q_2 has twice the W/L ratio of Q_1. If v_{id} is a small sine-wave signal and $k_n=\mu_n C_{ox}$, find:
   (a) I_{D1} and I_{D2} in terms of I (4%)
   (b) V_{ov} ($=V_{GS}-V_{TH}$) for each of Q_1 and Q_2 in terms of I, k_n, and W/L (4%)
   (c) The differential gain A_d ($=V_{od}/V_{id}$) in terms of R_D, I, and V_{ov} (4%)

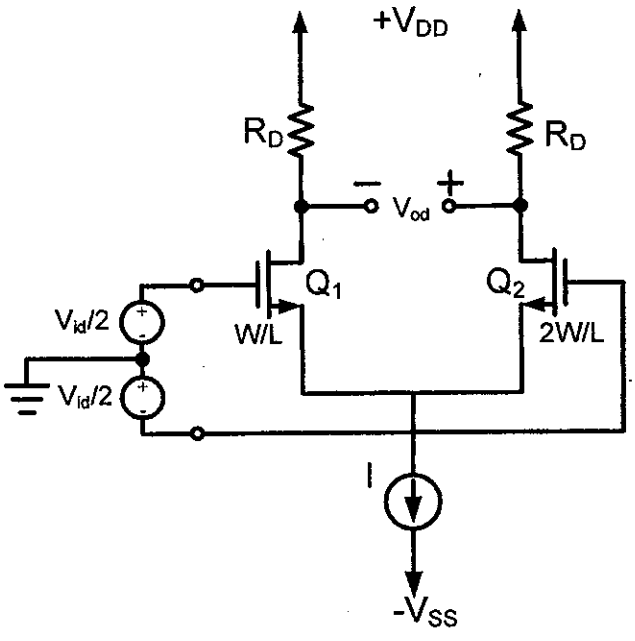

Fig. 6

8. Find the midband gain A_M (5%) and the upper 3-dB frequency f_H (5%) of a CS amplifier (Fig. 7) fed with a signal source having an internal resistance R_{sig}=10 kΩ. The amplifier has R_G=4.7 MΩ, R_D=R_L=20 kΩ, g_m=1mA/V, r_o=100 kΩ, C_{gs}=1 pF, and C_{gd}=0.4 pF.

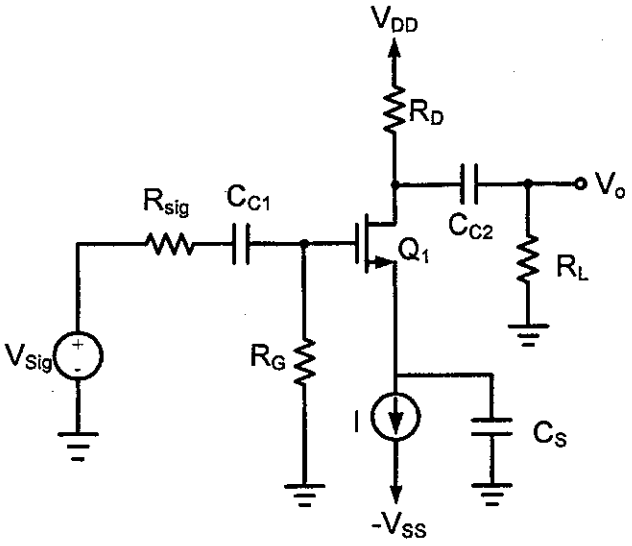

Fig. 7

9. Considering the transresistance amplifier with feedback as shown in Fig. 8, if g_m=5 mA/V, r_o=50 kΩ, R_f=10 kΩ, and R_s=2 kΩ
   (a) Find open-loop voltage gain A (4%)
   (b) Find the closed-loop gain $A_f = V_o/I_S$ (4%)
   (c) Find the input resistance R_{in} (4%)
   (d) Find the output resistance R_{out} (4%)

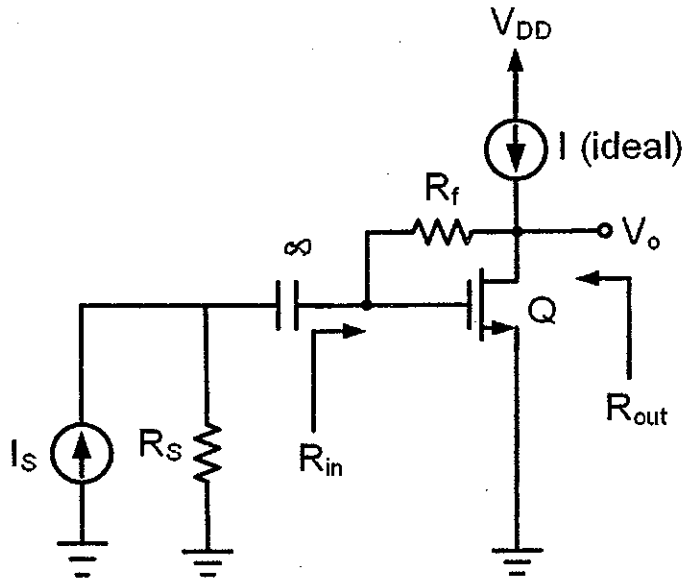

Fig. 8