編號： 179、198

# 國立成功大學 108 學年度碩士班招生考試試題

系　　所：電機工程學系 電機資訊學院-微電、奈米聯招

考試科目：電子學

考試日期：0223，節次：1



※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. The circuit of Fig. 1 is used to create an ac-coupled noninverting amplifier with a gain of 100 V/V using resistor $R_2$ of 100 kΩ.
   (a) What values of $R_1$ and $R_3$ should be used ? (4%)
   (b) For break frequency due to $C_1$ at 100 Hz, and that due to $C_2$ at 10 Hz, what values of $C_1$ and $C_2$ are needed ?(8%)

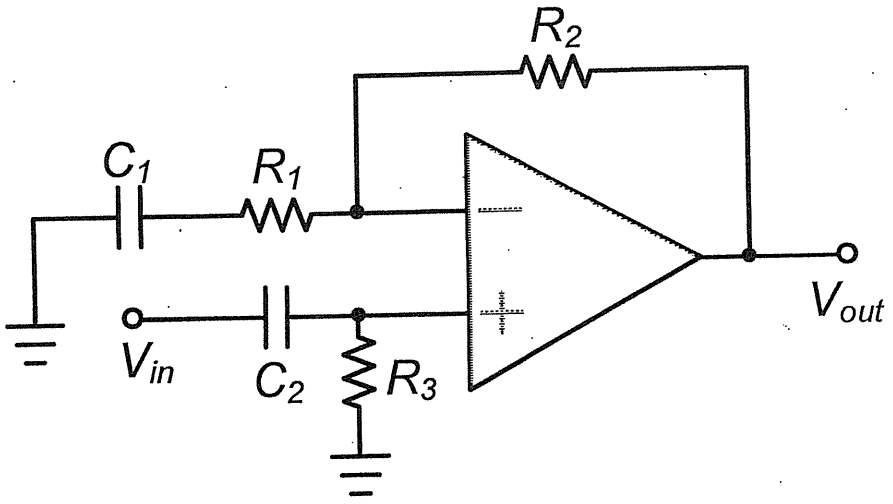


**Fig. 1**

2. Consider an operational rectifier as shown in Fig. 2 with R=1 kΩ. Assume that the op amp is ideal and that its output saturates at ±12 V. The diode has a 0.7-V drop at 1-mA current. Find the voltages ($V_A$ and $V_O$) that result at the rectifier output ($V_O$) and at the opamp output ($V_A$) under the conditions:
   (a) $V_I$=10mV (4%)
   (b) $V_I$=1V (4%)
   (c) $V_I$=-1V (4%)

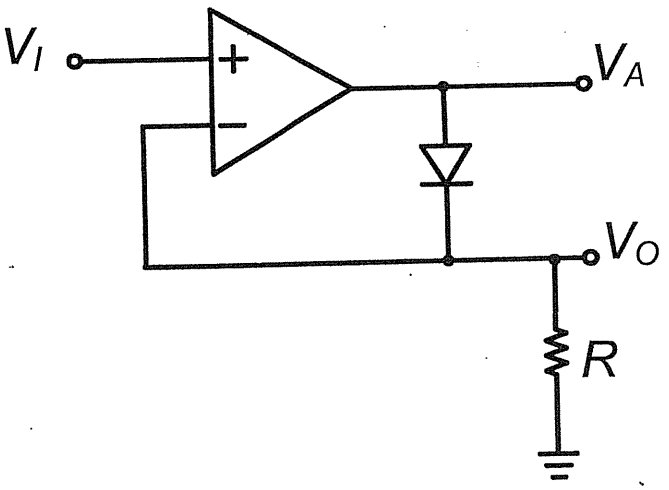


**Fig. 2**

3. The CMOS cascade differential amplifier of Fig. 3 is fabricated in a 0.18-μm technology for which $\mu_n C_{ox}=4\mu_p C_{ox}=400\ \mu A/V^2$, $|V_t|=0.5V$, and $|V_A'|=10\ V/\mu m$. Assume the bias current I=100μA, and all transistors have a channel length twice the minimum length and are operating at $|V_{ov}|=|V_{GS}-V_t|=0.2V$.
   (a) Find W/L for each of $Q_1$ to $Q_4$ (4%)
   (b) Find W/L for each of $Q_5$ to $Q_8$ (4%)
   (c) Determine the differential voltage gain $A_d(=v_{od}/v_{id})$ (4%)

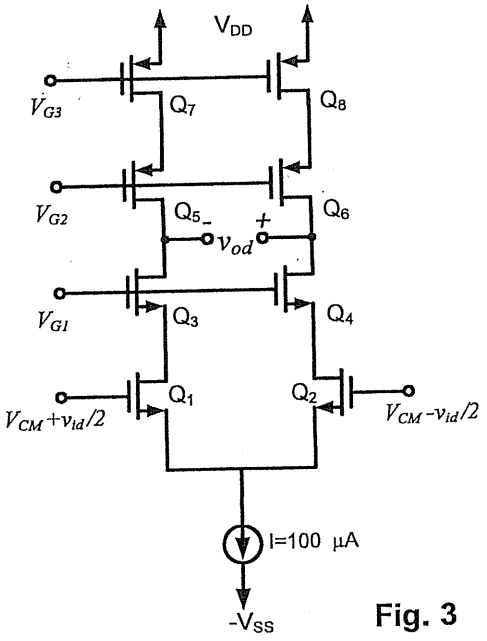


Fig. 3

4. As shown in Fig. 4, all the MOS transistors in the feedback are sized to operate at $|V_{OV}|=|V_{GS}-V_t|=0.2$ V. For all transistors, $|V_t|=0.4V$ and early voltage=$|V_A|=|1/\lambda|=20V$.
   (a) Find the closed-loop gain of $A_f$ $(=I_o/V_S)$. (4%)
   (b) Find the output impedance, $R_{out}$. (5%)
   (c) If the voltage at the source of $Q_5$ is taken as the output ($V_o$), find the voltage gain $(V_O/V_S)$ using the value of $I_o/V_S$ obtained in (a). (5%)

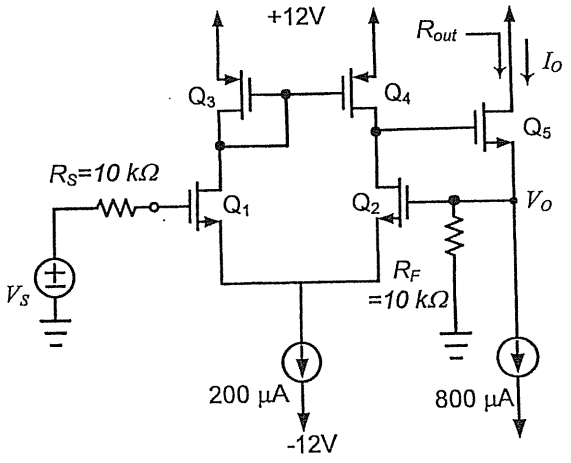


Fig. 4

5. Explanatory questions:
   (a) Draw and explain the circuit diagram of a basic Wien-bridge oscillator. (5%)
   (b) A student mistakenly configures a Sallen and Key filter as shown in Fig. 5. Explain why this is not a useful circuit. (5%)

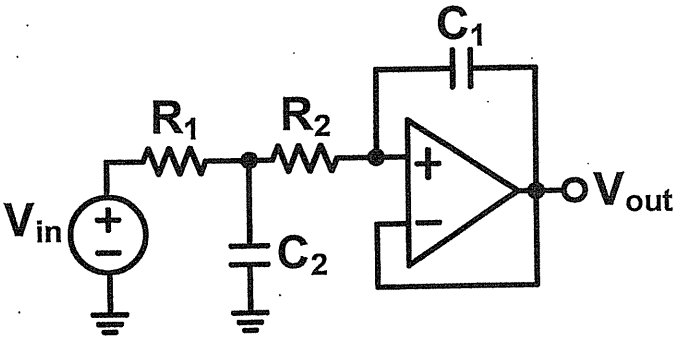


Fig. 5

6. Consider a three-pole feedback amplifier with a loop gain function given by

$$T(f) = \frac{1000}{(1+j\frac{f}{10^4})(1+j\frac{f}{10^6})(1+j\frac{f}{10^8})}$$

   (a) Please draw the Bode plot of this amplifier. (5%)
   (b) Insert an additional dominant pole (assuming all original poles do not change) such that the resulting phase margin is at least 45 degrees. (5%)

7. Consider the circuit shown in Fig. 6. Assume the saturated output voltages of op-amp are ±10V.
   (a) Find $R_x$ such that the frequency of oscillation is 500 Hz when the potentiometer is connected to point A. (5%)
   (b) Using the result of (a), determine the oscillator frequency when the potentiometer is connected to point B. (5%)

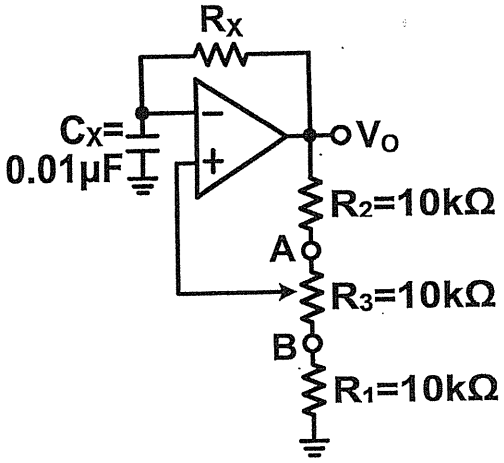


Fig. 6

8. For the op-amp circuit shown in Fig. 7, assume transistor parameters of $|V_T|$=0.5V (all transistors), $K_n'(=\mu_n C_{ox})$=100μA/V$^2$, $K_p'(=\mu_p C_{ox})$= 40μA/V$^2$, and circuit parameters of $V^+$=5 V, $V^-$=−5V, $R_{set}$=225 kΩ and $C_1$=2pF. Given that the width-to-length ratios of transistor $M_3/M_4$=6.25 and all other transistors have the same W/L ratios of 12.5.
   (a) Determine the dc bias currents of the input (i.e. $M_1/M_2$) and second (i.e. $M_7$) stages. (4%)
   (b) Assume $\lambda(=1/V_A)$=0.02V$^{-1}$ for all transistors, find the small-signal voltage gains of the input and second stages, and the overall voltage gain of the op-amp. (5%)
   (c) Calculate the slew rate of this op-amp. (3%)

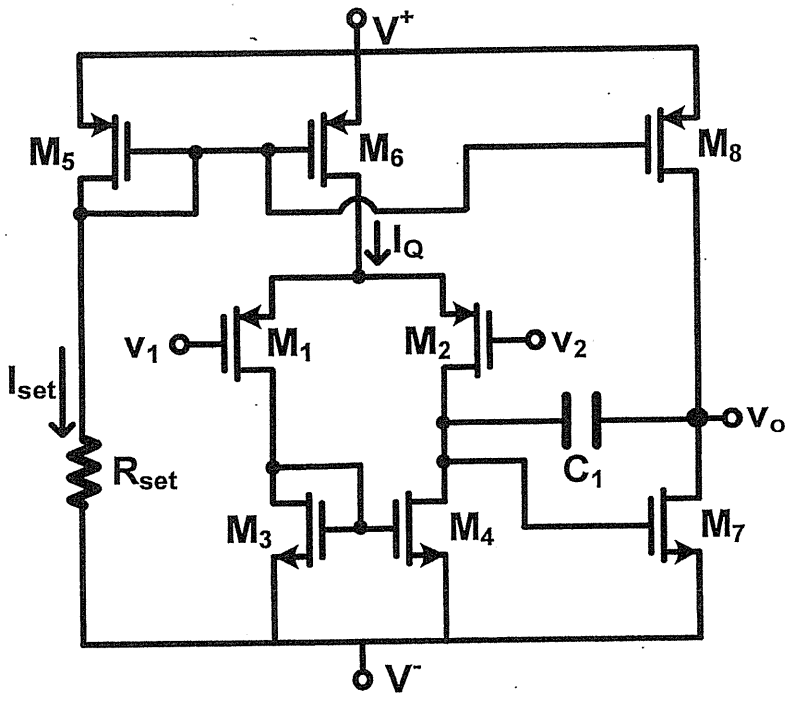


Fig. 7

9. Consider the switched-capacitor circuit shown in Fig. 8.
   (a) If the clock frequency is $f_C$=100 kHz and C=1.2 pF, what is the value of the simulated resistance? (4%)
   (b) A 50MΩ resistor is to be simulated using a clock frequency of $f_C$= 50 kHz. What is the required value of capacitor? (4%)

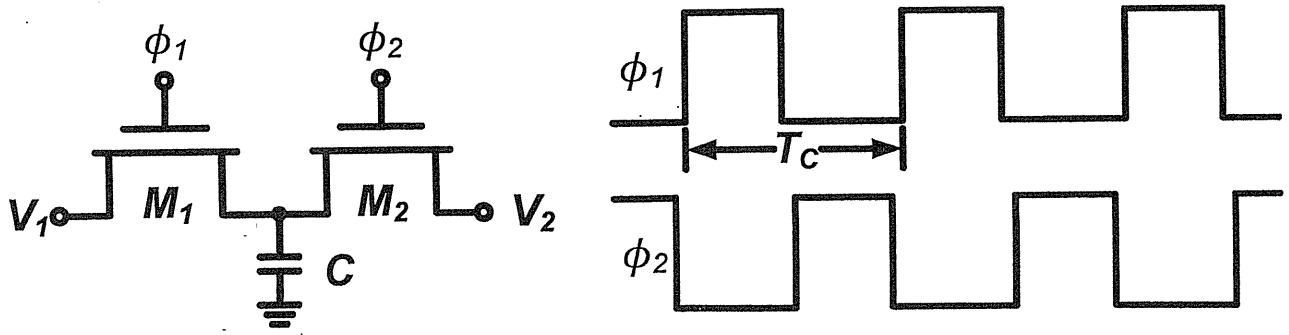


Fig. 8