國立成功大學

110學年度碩士班招生考試試題

編　號：179、197

系　所：電機工程學系
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科　目：電子學

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節　次：第 1 節

備　註：可使用計算機

※ 考生請注意：本試題可使用計算機。 請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. (選擇題，每小題 5 分) Please choose the most appropriate answer for the following questions:
   (1) Giving an amplifier with an open-loop gain of 80 dB and a feedback network with a feedback factor of 1/50. What is the closed-loop gain of the amplifier with the addition of the negative feedback?
   (a) 1.6 dB, (b) 16 dB, (c) 34 dB, (d) 46 dB.
   (2) An op amp that has a slew rate of 1 V/μs and a unity-gain bandwidth f_t of 1 MHz is connected in the unity-gain follower configuration. What is the largest possible input voltage step for which the output waveform will still be given by the exponential ramp, i.e. NOT slew-rate limited.
   (a) 0.16 V, (b) 0.32 V, (c) 1.6 V, (d) 3.2 V.
   (3) What is the value of the power-supply rejection ratio with respect to vdd ($PSRR^+ \equiv A_d / A^+$) for a well-matched two stage CMOS op amp, where g_m and r_o is the transconductance and output resistance of a MOSFET, respectively?
   (a) 0, (b) $\approx g_m r_o$, (c) $\approx (g_m r_o)^2$, (d) ∞.
   (4) For enhancing the common-mode rejection ratio (CMRR) of a two-stage CMOS op amp, we should
   (a) design larger channel length for transistors, and operate transistors at larger overdrive voltage,
   (b) design larger channel length for transistors, and operate transistors at smaller overdrive voltage,
   (c) design smaller channel length for transistors, and operate transistors at larger overdrive voltage,
   (d) design smaller channel length for transistors, and operate transistors at smaller overdrive voltage.
   (5) What is the theoretical power-conversion efficiency of an ideal class D output stage?
   (a) 25%, (b) 50%, (c) 78.5%, (d) 100%.
   (6) What will the collect current (I_C) be if we keep the voltage across the base-emitter junction (V_{BE}) constant and rise the temperature for a bipolar transistor?
   (a) increased, (b) decreased, (c) held constant, (d) unpredictable.
   (7) What is the equivalent impedance of a LC resonator when the inductor (with inductance L) and capacitor (with capacitance C) are connected in parallel and resonate at a frequency of $\omega = 1/\sqrt{LC}$?
   (a) 0, (b) C/L, (c) L/C, (d) ∞.
   (8) Let V_{OV} is the overdrive voltage at which two transistors operate when conducting drain currents equal to $I/2$, i.e. the equilibrium situation, for a MOSFET differential pair. For this differential pair, the current will be steered entirely into one of the two transistors when its differential voltage (v_{id}) reaches the value of
   (a) $V_{OV}/\sqrt{2}$, (b) $V_{OV}/(2-\sqrt{2})$, (c) $\sqrt{2}V_{OV}$, (d) $(2-\sqrt{2})V_{OV}$.
   (9) A multi-pole amplifier having a first pole at 1 MHz and an open-loop gain of 100 dB is to be compensated for closed-loop gain as low as 20 dB by the introduction of a new dominant pole. At what frequency must the new pole be placed?
   (a) 100 Hz, (b) 1 kHz, (c) 5 kHz, (d) 5 MHz.

(10) For the CD-CS amplifier configuration, the major purpose for adding the CD stage in the front of the CS amplifier is to
(a) raise the gain,
(b) increase the input resistance,
(c) decrease the output resistance,
(d) widen the bandwidth.

2. Fig. 1 shows the inverting amplifier with an ideal opamp with an input resistance of 100 kΩ. Use this circuit to design an inverting amplifier with a gain that can be varied from -1 V/V to -100 V/V using the 100-kΩ potentiometer R_4. Assume that for practical reasons it is required no to use resistors greater than 1MΩ.
(a) Derive an expression for the closed-loop gain v_O/v_I of the circuit. (4%)
(b) Find the required values, R_2 and R_3. (8%)
(c) What voltage gain results when the potentiometer is set exactly at its middle value (note: x=0.5)? (4%)

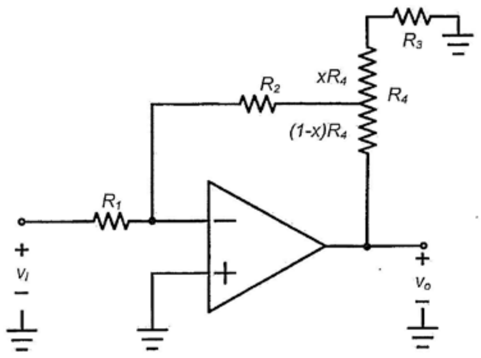

Fig. 1

3. A CS amplifier is shown in Fig. 2 with g_m=5 mA/V, C_{gs}=5 pF, C_{gd}=1 pF, C_L=5 pF, R_{sig}=10 kΩ, and R_L=10 kΩ.
(a) Find effective high-frequency time constant τ_H and the 3-dB frequency f_H? (8%)
(b) What is the percentage of τ_H that is caused by the interaction of R_{sig} with the effective input capacitance? (4%)
(c) To what value must R_{sig} be lowered in order to double f_H ? (4%)

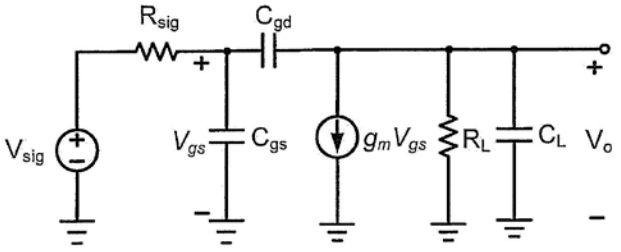

Fig. 2

4. The feedback transresistance amplifier in Fig. 3 utilizes two identical MOSFETs biased by ideal current sources I=0.4 mA. The MOSFETs are sized to operate at overdrive voltage $V_{ov}=V_{GS}-V_{tn}=0.2V$ and have threshold voltage $V_{tn}=0.5$ V and Early voltage $V_A=16$ V. The feedback resistance $R_F=10$ kΩ. The open loop gain and closed loop gain are A and A_f, respectively, and the feedback factor is β.
   (a) What is β? (2%)
   (b) Provide the A circuit and derive an expression for A in terms of g_{m1}, r_{o1}, g_{m2}, r_{o2} and R_F.(4%)
   (c) Find the values of A and $A_f \cong V_o/I_s$ for the component values given. (4%)
   (d) Find the expression and values of R_{in} and R_{out}. (8%)

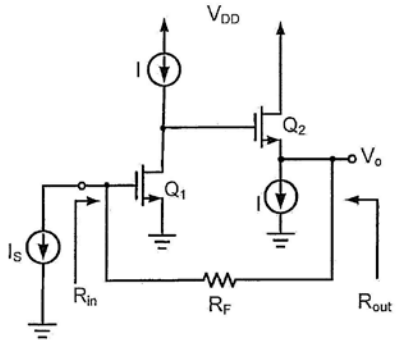

Fig. 3